XC9500XL High-Performance CPLD Family Data Sheet

DS054 (v2.4)

Product Specification

Features

- Optimized for high-performance 3.3V systems
  - 5 ns pin-to-pin logic delays, with internal system frequency up to 208 MHz
  - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
  - Pb-free available for all packages
  - Lower power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Supports hot-plugging capability
  - Full IEEE Std 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 10,000 program/erase cycles endurance rating
  - 20 year data retention
- Pin-compatible with 5V core XC9500 family in common package footprints

Table 1: **XC9500XL Device Family**

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
T_{PD} (ns)	5	5	5	6
T_{SU} (ns)	3.7	3.7	3.7	4.0
T_{CO} (ns)	3.5	3.5	3.5	3.8
f_{SYSTEM} (MHz)	178	178	178	208

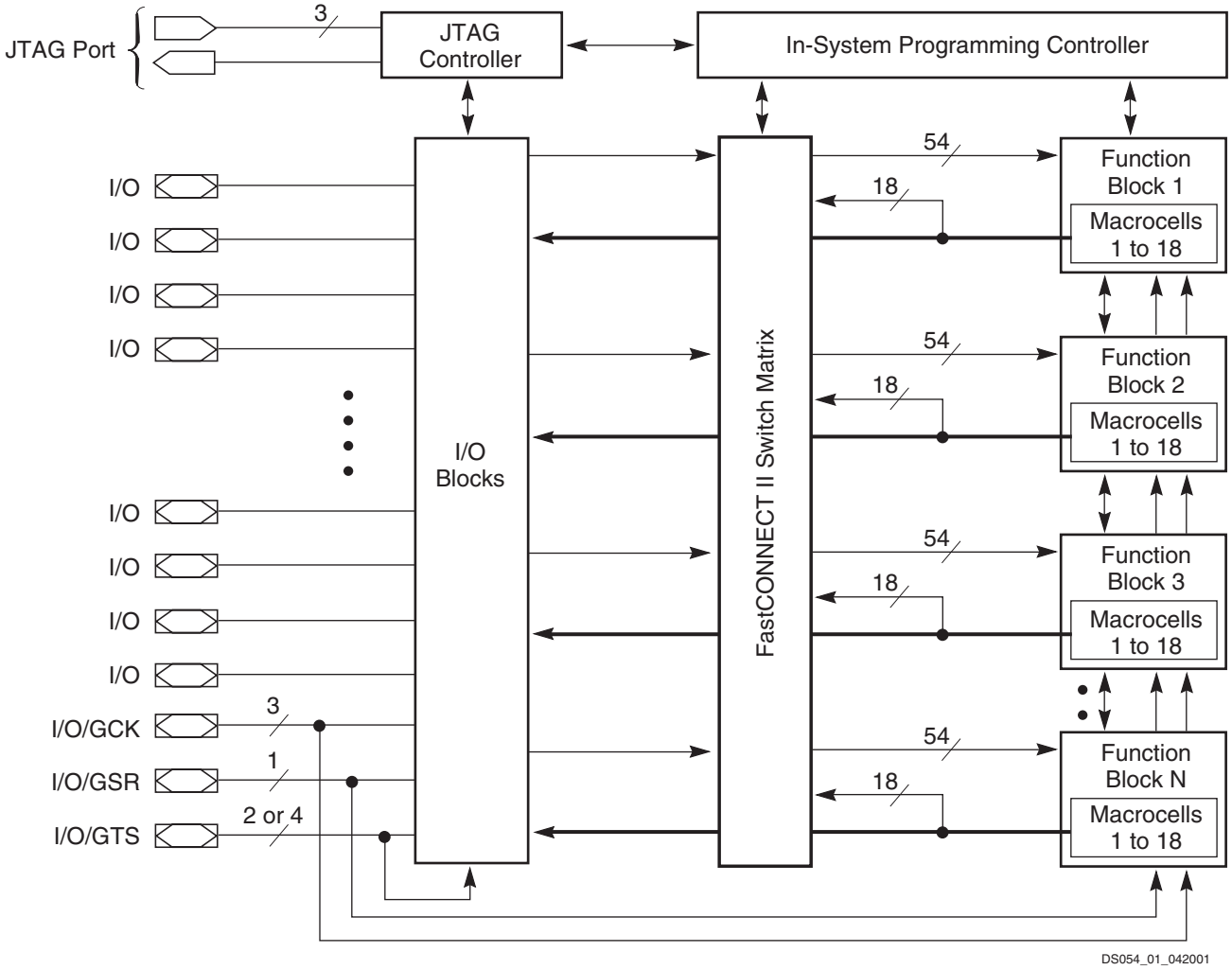

Figure 1: **XC9500XL Architecture**
Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

Family Overview

The FastFLASH XC9500XL family is a 3.3V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where high device reliability and low power dissipation is important. Each XC9500XL device supports in-system programming (ISP) and the full IEEE Std 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XL family is designed to work closely with the Xilinx® Virtex®, Spartan®-XL and XC4000XL FPGA families, allowing system designers to partition logic optimally between fast interface circuitry and high-density general purpose logic. As shown in Table 1, logic density of the XC9500XL devices ranges from 800 to 6400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500XL family members are fully pin-compatible, allowing easy design migration across multiple density options in a given package footprint.

The XC9500XL architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. In-system programming throughout the full commercial operating range and a high programming endurance rating provide worry-free reconfigurations of system field upgrades. Extended data retention supports longer and more reliable system operating life.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. Each user pin is compatible with 5V, 3.3V, and 2.5V inputs, and the outputs may be configured for 3.3V or 2.5V

operation. The XC9500XL device exhibits symmetric full 3.3V output voltage swing to allow balanced rise and fall times. Additional details can be found in the application notes listed in "Further Reading" on page 17.

Architecture Description

Each XC9500XL device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT II switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with extra wide 54inputs and 18 outputs. The FastCONNECT II switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, up to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1

Function Block

Each Function Block, as shown in Figure 2 is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Fifty-four inputs provide 108 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

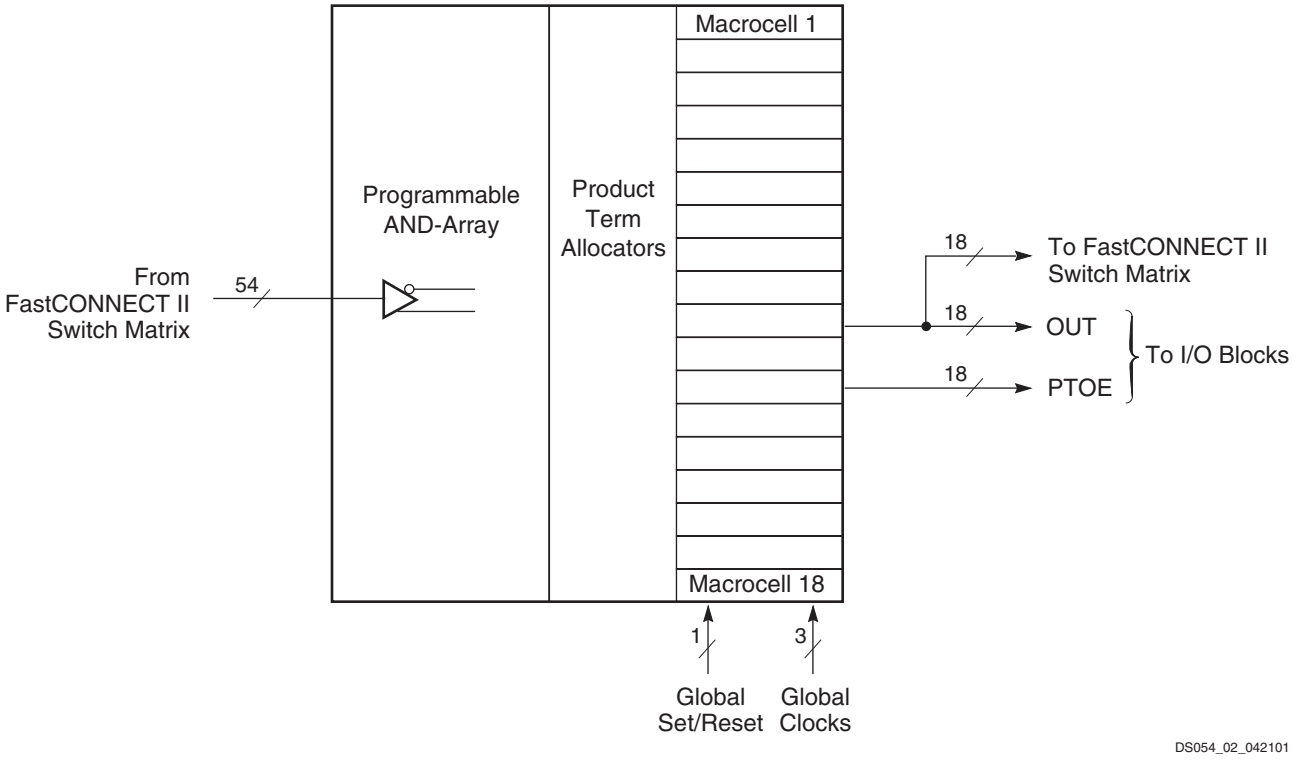

Figure 2: **XC9500XL Function Block**

Macrocell

Each XC9500XL macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, clock enable, set/reset, and output enable. The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).