5V, Byte Alterable EEPROM

The X28HC256 is a second generation high performance CMOS 32k x 8 EEPROM. It is fabricated with Intersil's proprietary, textured poly floating gate technology, providing a highly reliable 5V only nonvolatile memory.

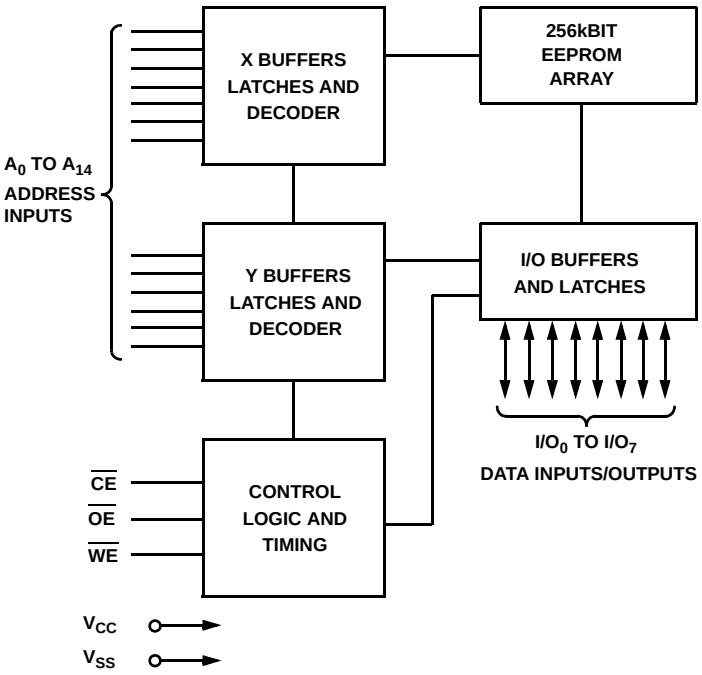
The X28HC256 supports a 128-byte page write operation, effectively providing a 24µs/byte write cycle, and enabling the entire memory to be typically rewritten in less than 0.8 seconds. The X28HC256 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, two methods of providing early end of write detection. The X28HC256 also supports the JEDEC standard Software Data Protection feature for protecting against inadvertent writes during power-up and power-down.

Endurance for the X28HC256 is specified as a minimum 1,000,000 write cycles per byte and an inherent data retention of 100 years.

Features

- Access time: 70ns
- Simple byte and page write
  - Single 5V supply
  - No external high voltages or V_{P-P} control circuits
  - Self-timed
  - No erase before write
  - No complex programming algorithms
  - No overerase problem
- Low power CMOS
  - Active: 60mA
  - Standby: 500µA
- Software data protection
  - Protects data against system level inadvertent writes
- High speed page write capability
- Highly reliable Direct Write™ cell
  - Endurance: 1,000,000 cycles
  - Data retention: 100 years
- Early end of write detection
  - DATA polling
  - Toggle bit polling
- Pb-free plus anneal available (RoHS compliant)

Block Diagram



Ordering Information (Continued)

PART NUMBER	PART MARKING	ACCESS TIME (ns)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X28HC256PIZ-12 (Note)	X28HC256PI-12 RRZ		-40 to +85	28 Ld PDIP (Pb-free)***	E28.6
X28HC256S-12*	X28HC256S-12 RR	120	0 to +70	28 Ld SOIC (300 mils)	MDP0027
X28HC256SZ-12 (Note)	X28HC256S-12 RRZ		0 to +70	28 Ld SOIC (300 mils) (Pb-free)	MDP0027
X28HC256SI-12*	X28HC256SI-12 RR		-40 to +85	28 Ld SOIC (300 mils)	MDP0027
X28HC256SIZ-12 (Note)	X28HC256SI-12 RRZ		-40 to +85	28 Ld SOIC (300 mils) (Pb-free)	MDP0027
X28HC256SM-12*, **	X28HC256SM-12 RR		-55 to +125	28 Ld SOIC (300 mils)	MDP0027
X28HC256D-90	X28HC256D-90 RR	90	0 to +70	28 Ld CERDIP (520 mils)	F28.6
X28HC256DI-90	X28HC256DI-90 RR		-40 to +85	28 Ld CERDIP (520 mils)	F28.6
X28HC256DM-90	X28HC256DM-90 RR		-55 to +125	28 Ld CERDIP (520 mils)	F28.6
X28HC256DMB-90	C X28HC256DMB-90		MIL-STD-883	28 Ld CERDIP (520 mils)	F28.6
X28HC256EM-90	X28HC256EM-90 RR		-55 to +125	32 Ld LCC (458 mils)	
X28HC256EMB-90	C X28HC256EMB-90		MIL-STD-883	32 Ld LCC (458 mils)	
X28HC256FI-90	X28HC256FI-90 RR		-40 to +85	28 Ld FLATPACK (440 mils)	
X28HC256FM-90	X28HC256FM-90 RR		-55 to +125	28 Ld FLATPACK (440 mils)	
X28HC256FMB-90	C X28HC256FMB-90		MIL-STD-883	28 Ld FLATPACK (440 mils)	
X28HC256J-90*	X28HC256J-90 RR		0 to +70	32 Ld PLCC	N32.45x55
X28HC256JZ-90* (Note)	X28HC256J-90 ZRR		0 to +70	32 Ld PLCC (Pb-free)	N32.45x55
X28HC256JI-90*	X28HC256JI-90 RR		-40 to +85	32 Ld PLCC	N32.45x55
X28HC256JIZ-90* (Note)	X28HC256JI-90 ZRR		-40 to +85	32 Ld PLCC (Pb-free)	N32.45x55
X28HC256JM-90*	X28HC256JM-90 RR		-55 to +125	32 Ld PLCC	N32.45x55
X28HC256KM-90	X28HC256KM-90 RR		-55 to +125	28 Ld PGA	G28.550x650A
X28HC256KMB-90	C X28HC256KMB-90		MIL-STD-883	28 Ld PGA	G28.550x650A
X28HC256P-90	X28HC256P-90 RR	90	0 to +70	28 Ld PDIP	E28.6
X28HC256PZ-90 (Note)	X28HC256P-90 RRZ		0 to +70	28 Ld PDIP (Pb-free)***	E28.6
X28HC256PI-90	X28HC256PI-90 RR		-40 to +85	28 Ld PDIP	E28.6
X28HC256PIZ-90 (Note)	X28HC256PI-90 RRZ		-40 to +85	28 Ld PDIP (Pb-free)**	E28.6
X28HC256S-90*	X28HC256S-90 RR		0 to +70	28 Ld SOIC (300 mils)	MDP0027
X28HC256SI-90*	X28HC256SI-90 RR		-40 to +85	28 Ld SOIC (300 mils)	MDP0027
X28HC256SIZ-90 (Note)	X28HC256SI-90 RRZ		-40 to +85	28 Ld SOIC (300 mils) (Pb-free)	MDP0027
X28HC256SI-20T1		200	-40 to +85	28 Ld SOIC (300 mils) Tape and Reel	MDP0027

*Add "T1" suffix for tape and reel.

**Add "T2" suffix for tape and reel.

***Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Temperature Under Bias . . . . . .-10°C to +85°C
X28HC256 . . . . . .-65°C to +135°C
X28HC256I, X28HC256M . . . . . .-65°C to +150°C
Voltage on any Pin with Respect to V_{SS} . . . . . -1V to +7V
DC Output Current 10mA

Operating Conditions

Temperature Range . . . . . .
Commerical . . . . . 0°C to +70°C
Industrial. . . . . .-40°C to +85°C
Military . . . . . .-55°C to +125°C
Supply Voltage . . . . . 5V ± 10%

Thermal Information

Storage Temperature . . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications Over Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP (Note 7)	MAX	
V_{CC} Active Current (TTL Inputs)	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = open, address inputs = .4V/2.4V levels @ f = 10MHz		30	60	mA
V_{CC} Standby Current (TTL Inputs)	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, All I/O's = open, other inputs = V_{IH}		1	2	mA
V_{CC} Standby Current (CMOS Inputs)	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.3V, $\overline{OE}$ = GND, All I/Os = open, other inputs = V_{CC} - 0.3V		200	500	µA
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CC}			10	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}			10	µA
Input LOW Voltage	V_{IL} (Note 2)		-1		0.8	V
Input HIGH Voltage	V_{IH} (Note 2)		2		V_{CC} + 1	V
Output LOW Voltage	V_{OL}	I_{OL} = 6mA			0.4	V
Output HIGH Voltage	V_{OH}	I_{OH} = -4mA	2.4			V

NOTES:

1. Typical values are for T_A = +25°C and nominal supply voltage.
2. V_{IL} min. and V_{IH} max. are for reference only and are not tested.

Power-up Timing

PARAMETER	SYMBOL	MAX	UNIT
Power-up to read	t_{PUR}, Note 3	100	µs
Power-up to write	t_{PUW}, Note 3	5	ms

NOTE:

3. This parameter is periodically sampled and not 100% tested.

Capacitance T_A = +25°C, f = 1MHz, V_{CC} = 5V.

SYMBOL	TEST	CONDITIONS	MAX	UNIT
$C_{I/O}$ (Note 9)	Input/output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN} (Note 9)	Input capacitance	V_{IN} = 0V	6	pF

Endurance and Data Retention

PARAMETER	MIN	MAX	UNIT
Endurance	1,000,000		Cycles
Data retention	100		Years

AC Conditions of Test

Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

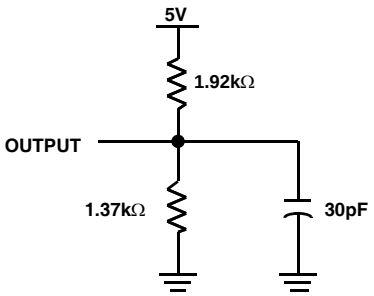
Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Mode Selection

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
L	L	H	Read	D_{OUT}	active
L	H	L	Write	D_{IN}	active
H	X	X	Standby and write inhibit	High Z	standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

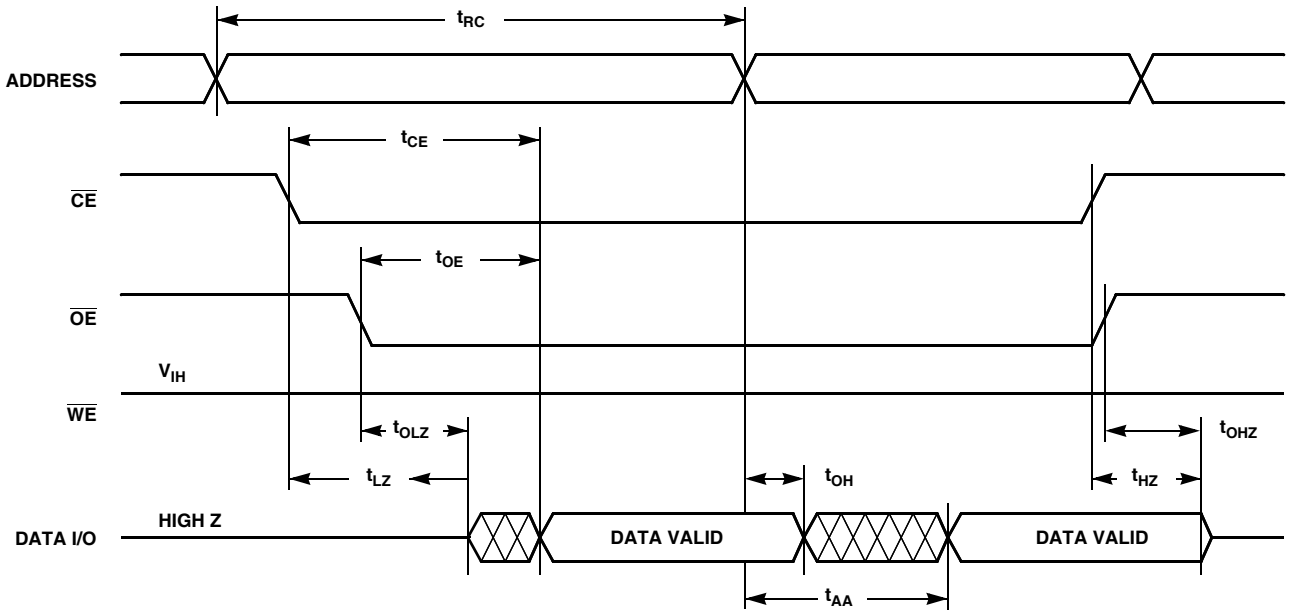
Equivalent AC Load Circuit



AC Electrical Specifications Over Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	SYMBOL	X28HC256-70		X28HC256-90		X28HC256-12		X28HC256-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{RC} (Note 5)	70		90		120		150		ns
Chip Enable Access Time	t_{CE} (Note 5)		70		90		120		150	ns
Address Access Time	t_{AA} (Note 5)		70		90		120		150	ns
Output Enable Access Time	t_{OE}		35		40		50		50	ns
$\overline{CE}$ LOW to Active Output	t_{LZ} (Note 4)	0		0		0		0		ns
$\overline{OE}$ LOW to Active Output	t_{OLZ} (Note 4)	0		0		0		0		ns
$\overline{CE}$ HIGH to High Z Output	t_{HZ} (Note 4)		35		40		50		50	ns
$\overline{OE}$ HIGH to High Z Output	t_{OHZ} (Note 4)		35		40		50		50	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		ns

Read Cycle



NOTES:

4. t_{LZ} min., t_{HZ}, t_{OLZ} min. and t_{OHZ} are periodically sampled and not 100% tested, t_{HZ} and t_{OHZ} are measured with C_L = 5pF, from the point when $\overline{CE}$, $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.
5. For faster 256k products, refer to X28VC256 product line.

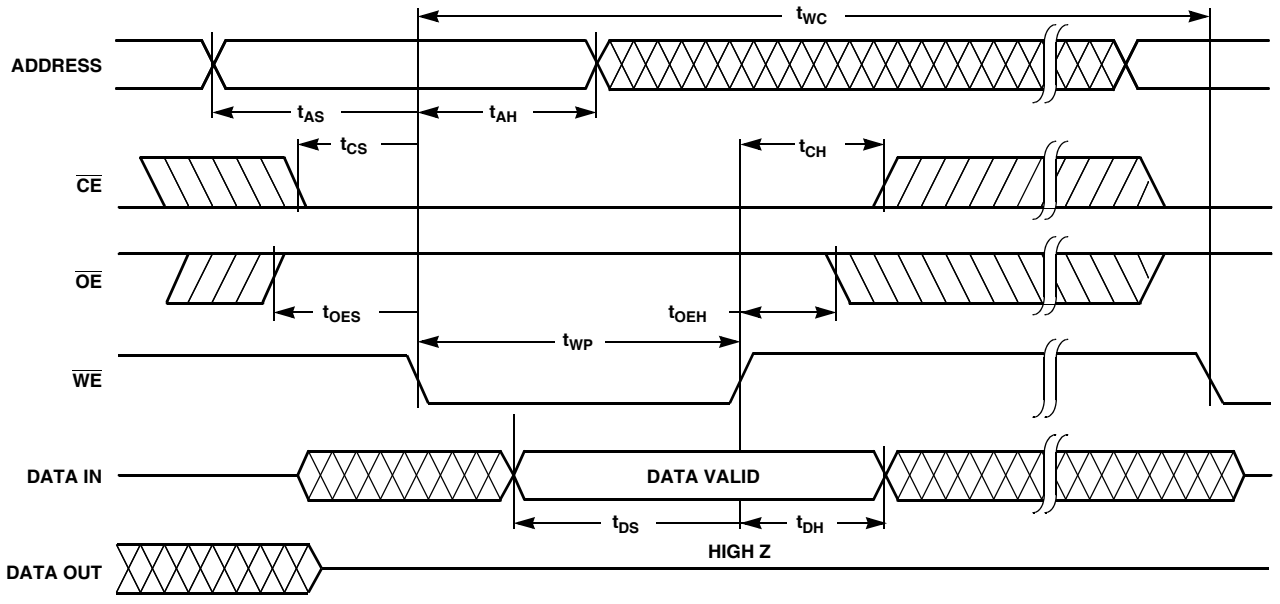
Write Cycle Limits

PARAMETER	SYMBOL	MIN	TYP (Note 6)	MAX	UNIT
Write Cycle Time	t_{WC} (Note 7)		3	5	ms
Address Setup Time	t_{AS}	0			ns
Address Hold Time	t_{AH}	50			ns
Write Setup Time	t_{CS}	0			ns
Write Hold Time	t_{CH}	0			ns
$\overline{CE}$ Pulse Width	t_{CW}	50			ns
$\overline{OE}$ HIGH Setup Time	t_{OES}	0			ns
$\overline{OE}$ HIGH Hold Time	t_{OEH}	0			ns
$\overline{WE}$ Pulse Width	t_{WP}	50			ns
$\overline{WE}$ HIGH Recovery (page write only)	t_{WPH} (Note 8)	50			ns
Data Valid	t_{DV}			1	µs
Data Setup	t_{DS}	50			ns
Data Hold	t_{DH}	0			ns
Delay to Next Write After Polling is True	t_{DW} (Note 8)	10			µs
Byte Load Cycle	t_{BLC}	0.15		100	µs

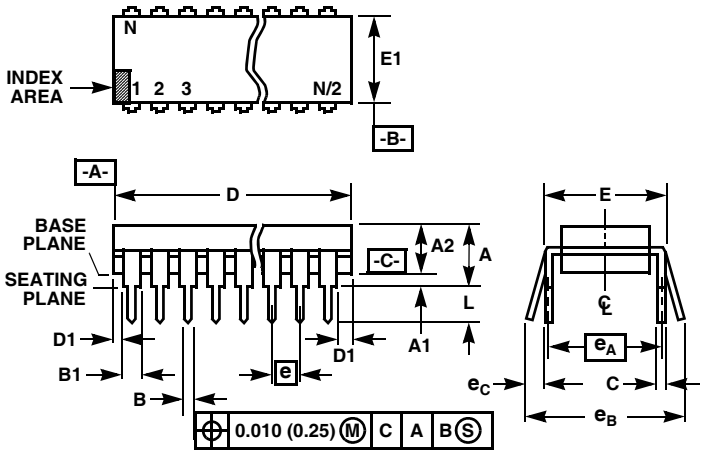
NOTES:

6. Typical values are for T_A = +25°C and nominal supply voltage.
7. t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
8. t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{WE}$ Controlled Write Cycle



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

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