M48T02
M48T12

## 5.0 V, 16 Kbit (2 Kb x 8) TIMEKEEPER® SRAM

Features

■ Integrated, ultra low power SRAM, real time clock, and power-fail control circuit

■ BYTEWIDE™ RAM-like clock access

■ BCD coded year, month, day, date, hours, minutes, and seconds

■ Typical clock accuracy of ±1 minute a month, at 25°C

■ Software controlled clock calibration for high accuracy applications

■ Automatic power-fail chip deselect and WRITE protection

■ WRITE protect voltages
  (V_{PFD} = Power-fail deselect voltage):
  – M48T02: V_{CC} = 4.75 to 5.5 V
    $4.5\ V \leq V_{PFD} \leq 4.75\ V$
  – M48T12: V_{CC} = 4.5 to 5.5 V
    $4.2\ V \leq V_{PFD} \leq 4.5\ V$

■ Self-contained battery and crystal in the CAPHAT™ DIP package

■ Pin and function compatible with JEDEC standard 2 K x 8 SRAMs

■ RoHS compliant
  – Lead-free second level interconnect
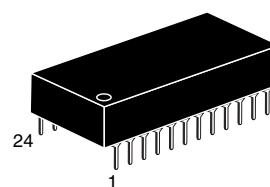
PCDIP24 (PC)
battery/crystal
CAPHAT™

1   Description

The M48T02/12 TIMEKEEPER® RAM is a 2 Kb x 8 non-volatile static RAM and real time clock which is pin and functional compatible with the DS1642.

A special 24-pin, 600 mil DIP CAPHAT™ package houses the M48T02/12 silicon with a quartz crystal and a long life lithium button cell to form a highly integrated battery backed-up memory and real-time clock solution.

The M48T02/12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48T02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2 Kb x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

Figure 1.   Logic diagram

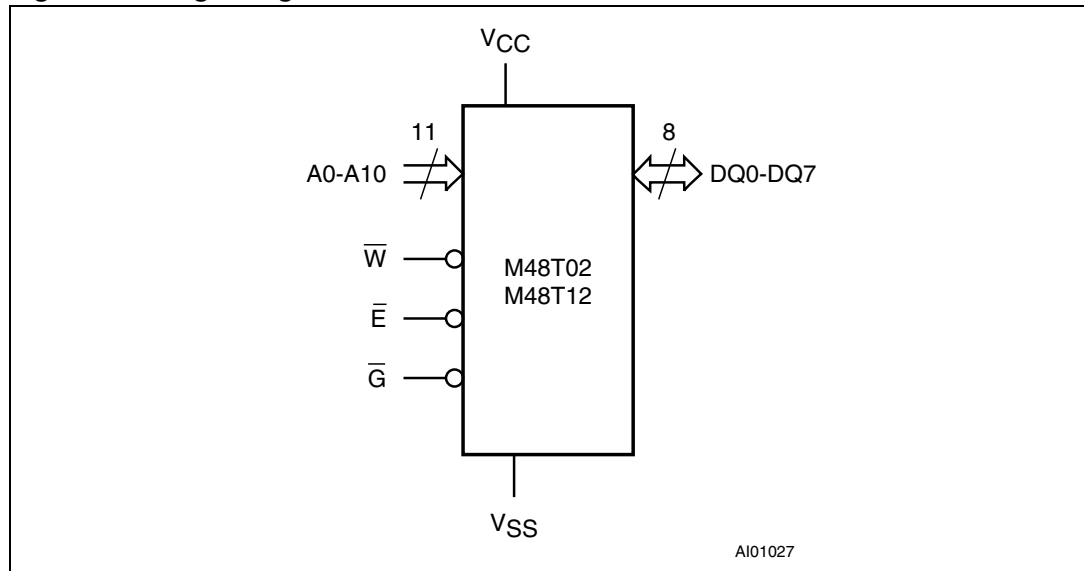**Table 1.   Signal names**

A0-A10	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{E}$	Chip enable
$\overline{G}$	Output enable
$\overline{W}$	WRITE enable
V_{CC}	Supply voltage
V_{SS}	Ground

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for output data hold time (t_{AXQX}) but will go indeterminate until the next address access.

Figure 4.   Read mode AC waveforms
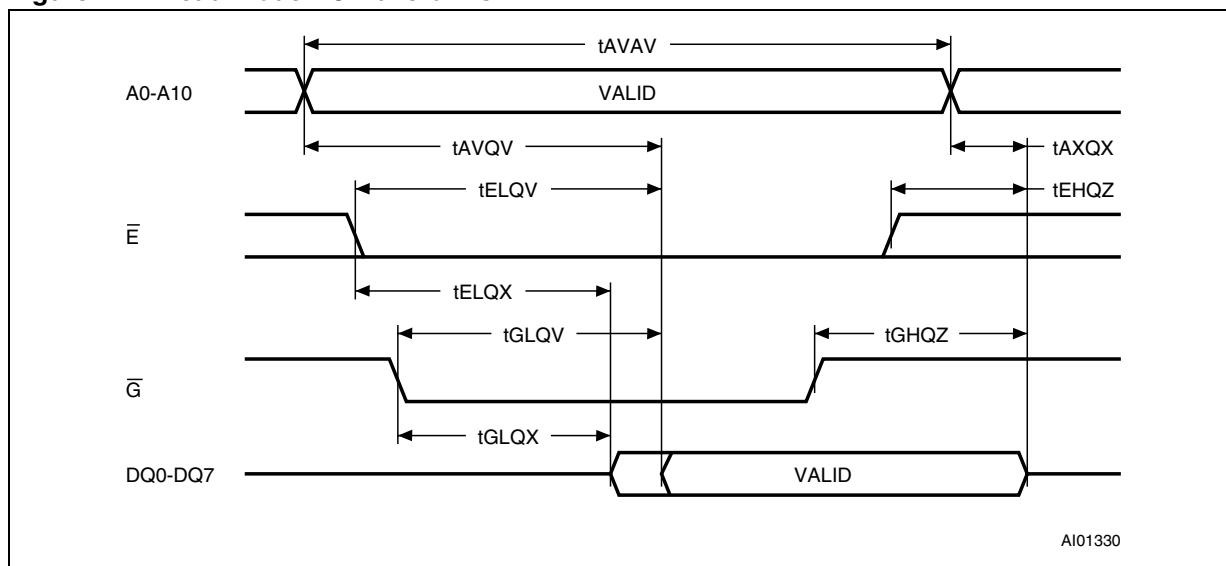
Note: WRITE enable ($\overline{W}$) = High.

Table 3.   Read mode AC characteristics

| Symbol | Parameter[1] | M48T02/M48T12 | | | | | | Unit |
| | | −70 | | −150 | | −200 | | |
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	READ cycle time	70		150		200		ns
t_{AVQV}	Address valid to output valid		70		150		200	ns
t_{ELQV}	Chip enable low to output valid		70		150		200	ns
t_{GLQV}	Output enable low to output valid		35		75		80	ns
t_{ELQX}	Chip enable low to output transition	5		10		10		ns
t_{GLQX}	Output enable low to output transition	5		5		5		ns
t_{EHQZ}	Chip enable high to output Hi-Z		25		35		40	ns
t_{GHQZ}	Output enable high to output Hi-Z		25		35		40	ns
t_{AXQX}	Address transition to output transition	10		5		5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

Table 4.   Write mode AC characteristics

Symbol	Parameter[1]	M48T02/M48T12						Unit
		−70		−150		−200		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	
t_{AVAV}	WRITE cycle time	70		150		200		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		0		ns
t_{AVEL}	Address valid to chip enable low	0		0		0		ns
t_{WLWH}	WRITE enable pulse width	50		90		120		ns
t_{ELEH}	Chip enable low to chip enable high	55		90		120		ns
t_{WHAX}	WRITE enable high to address transition	0		10		10		ns
t_{EHAX}	Chip enable high to address transition	0		10		10		ns
t_{DVWH}	Input valid to WRITE enable high	30		40		60		ns
t_{DVEH}	Input valid to chip enable high	30		40		60		ns
t_{WHDX}	WRITE enable high to input transition	5		5		5		ns
t_{EHDX}	Chip enable high to input transition	5		5		5		ns
t_{WLQZ}	WRITE enable low to output Hi-Z		25		50		60	ns
t_{AVWH}	Address valid to WRITE enable high	60		120		140		ns
t_{AVEH}	Address valid to chip enable high	60		120		140		ns
t_{WHQX}	WRITE enable high to output transition	5		10		10		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

2.3   Data retention mode

With valid V_{CC} applied, the M48T02/12 operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: *A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F The M48T02/12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.*

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal battery not oK ($\overline{BOK}$) flag will be set. The $\overline{BOK}$ flag can be checked after power up. If the $\overline{BOK}$ flag is set, the first WRITE attempted will be blocked. The flag is automatically cleared after the first WRITE, and normal RAM operation resumes. *Figure 7 on page 11* illustrates how a $\overline{BOK}$ check routine could be structured.

For more information on a battery storage life refer to the application note AN1012.

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6.   Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature	0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–40 to 85	°C
T_{SLD}[1]	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to 7	V
V_{CC}	Supply voltage	–0.3 to 7	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

5   DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 7.   Operating and AC measurement conditions

Parameter	M48T02	M48T12	Unit
Supply voltage (V_{CC})	4.75 to 5.5	4.5 to 5.5	V
Ambient operating temperature (T_A)	0 to 70	0 to 70	°C
Load capacitance (C_L)	100	100	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.
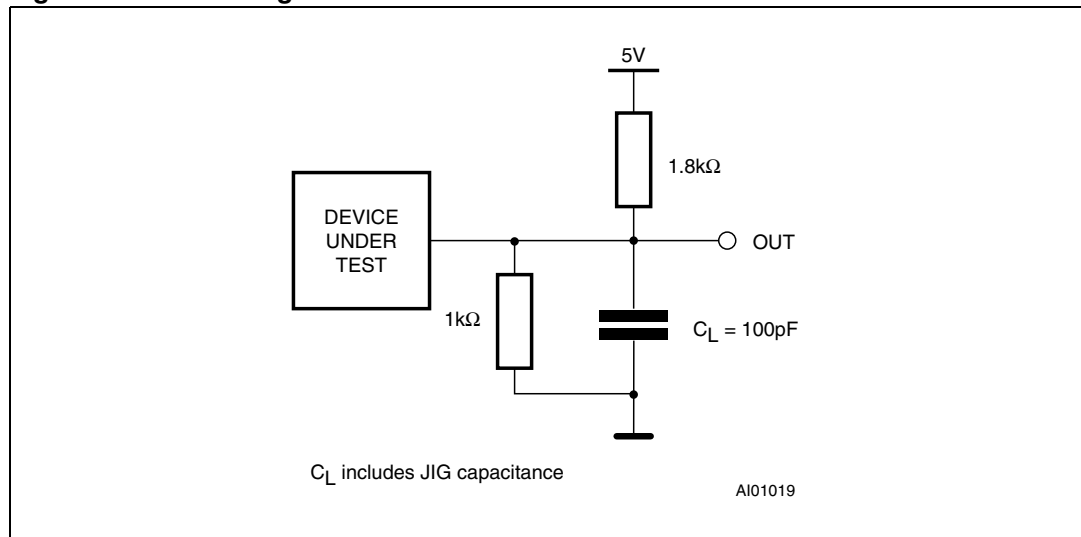
Figure 11.   AC testing load circuit

Table 8.   Capacitance

| Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		10	pF
C_{IO}[3]	Input / output capacitance		10	pF

1. Effective capacitance measured with power supply at 5 V. Sampled only, not 100% tested.

2. At 25°C, f = 1 MHz.

3. Outputs deselected.

Table 9.   DC characteristics

Symbol	Parameter	Test condition[1]	Min	Max	Unit
I_{LI}	Input leakage current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO}[2]	Output leakage current	$0V \leq V_{OUT} \leq V_{CC}$		±1	µA
I_{CC}	Supply current	Outputs open		80	mA
I_{CC1}[3]	Supply current (standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}[3]	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2\ V$		3	mA
V_{IL}	Input low voltage		−0.3	0.8	V
V_{IH}	Input high voltage		2.2	$V_{CC} + 0.3$	V
V_{OL}	Output low voltage	$I_{OL} = 2.1\ mA$		0.4	V
V_{OH}	Output high voltage	$I_{OH} = -1\ mA$	2.4		V

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

2. Outputs deselected.

3. Measured with control bits set as follows: R = '1'; W, ST, FT = '0.'

Figure 12.   Power down/up mode AC waveforms
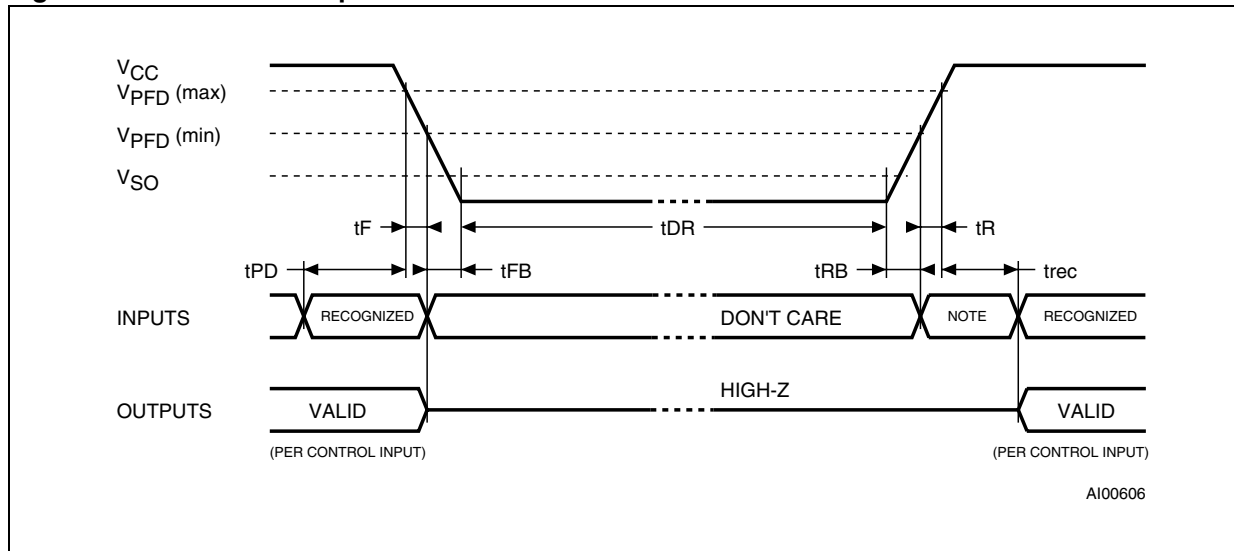
Note: *Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD} (min). Some systems may perform inadvertent WRITE cycles after V_{CC} rises above V_{PFD} (min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system clock is running.*

Table 10.   Power down/up AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power down	0		µs
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time	300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time	0		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time	1		µs
t_{rec}	$\overline{E}$ or $\overline{W}$ at V_{IH} before power-up	2		ms

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).

3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

**Table 11.   Power down/up trip points DC characteristics**

Symbol	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48T02	4.5	4.6	4.75	V
		M48T12	4.2	4.3	4.5	V
V_{SO}	Battery backup switchover voltage			3.0		V
t_{DR}[3]	Expected data retention time		10			YEARS

1. All voltages referenced to V_{SS}.

2. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.75 to 5.5 V or 4.5 to 5.5 V (except where noted).

3. At 25°C; V_{CC} = 0 V.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 13. PCDIP24 – 24-pin plastic DIP, battery CAPHAT™, package outline
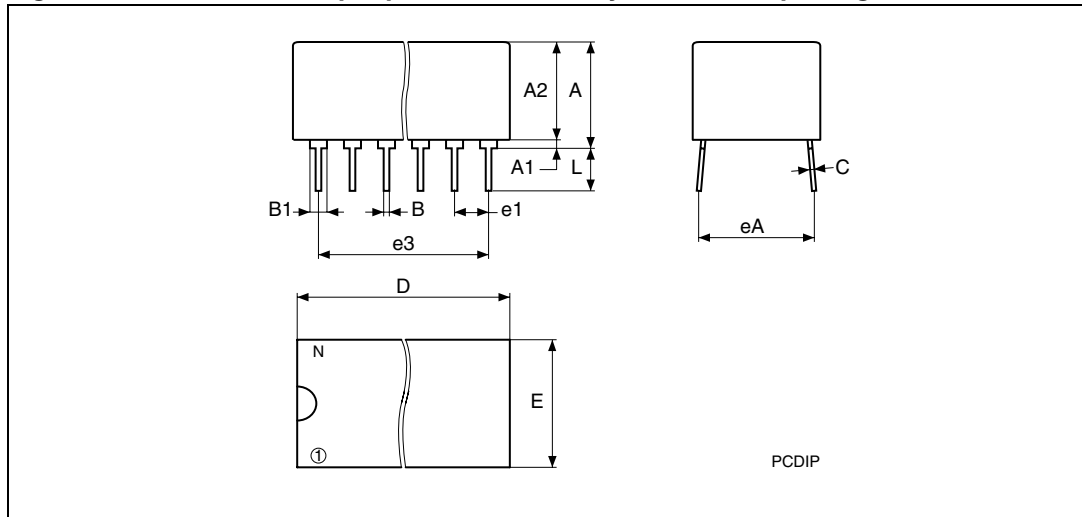
Note: *Drawing is not to scale.*

Table 12. PCDIP24 – 24-pin plastic DIP, battery CAPHAT™, package mech. data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N		24			24	

7   Part numbering

Table 13.   Ordering information scheme

Example: M48T   02   –70   PC   1

Device type

M48T

Supply voltage and write protect voltage

02 = V_{CC} = 4.75 to 5.5 V; V_{PFD} = 4.5 to 4.75 V

12 = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

Speed

–70 = 100 ns (M48T02/12)

–150 = 150 ns (M48T02/12)

–200 = 200 ns (M48T02/12)

Package

PC = PCDIP24

Temperature range

1 = 0 to 70°C

Shipping method

blank = ECOPACK® package, tubes

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.