

MAX635, MAX636, MAX637

Preset/Adjustable Output CMOS Inverting Switching Regulators

Evaluation Kits

none

Reliability Reports

Show FIT data for:

Request Reliability Report for:

Software/Models

none

Ordering Information

Notes:

1. Other options and links for purchasing parts are listed at:
2. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
3. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [Full Data Sheet](#) or [Part Naming Conventions](#).
4. * Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses. Note that "+", "#", "-" in the part number suffix describes RoHS status. Package drawings may show a different suffix character.

Devices: 1-77 of 77

MAX635	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX635ACJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX635BCJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX635BEJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX635AEJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis

MAX636ACSA+T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX636AESA			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX636AESA+			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX636AESA+T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX636AESA-T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX636BESA			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX637	Free Sample	Buy	Package: TYPE PINS FOOTPRINT DRAWING CODE/VAR*	Temp	RoHS/Lead-Free? Materials Analysis
MAX637ACJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637BCJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637AEJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX637BEJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX637BMJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-55°C to +125°C	RoHS/Lead-Free: No Materials Analysis
MAX637AMJA			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-55°C to +125°C	RoHS/Lead-Free: No Materials Analysis
MAX637AMJA/HR			Ceramic DIP; 8 pin; Dwg: 21-0045 (PDF) Use pkgcode/variation: J8-2*	-55°C to +125°C	RoHS/Lead-Free: No Materials Analysis
MAX637AC/D					See data sheet
MAX637ACPA+			PDIP; 8 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P8+2*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX637ACPA			PDIP; 8 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P8-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637BCPA			PDIP; 8 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P8-2*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637AEPA+			PDIP; 8 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P8+2*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX637AEPA			PDIP; 8 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P8-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX637BEPA			PDIP; 8 pin; Dwg: 21-0043 (PDF) Use pkgcode/variation: P8-2*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis

MAX637BCSA-T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637BESA-T				-40°C to +85°C	See data sheet
MAX637ACSA			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637ACSA+			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX637ACSA+T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	0°C to +70°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX637ACSA-T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637BCSA			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	0°C to +70°C	RoHS/Lead-Free: No Materials Analysis
MAX637AESA+T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX637AESA			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX637AESA+			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8+4*	-40°C to +85°C	RoHS/Lead-Free: Lead Free Materials Analysis
MAX637AESA-T			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis
MAX637BESA			SOIC; 8 pin; Dwg: 21-0041 (PDF) Use pkgcode/variation: S8-4*	-40°C to +85°C	RoHS/Lead-Free: No Materials Analysis

Notes and Comments

- Preset, or adjustable output (with 2 resistors)
- Preset: -5V (MAX635)
- -12V (MAX636)
- -15V (MAX637)



Preset/Adjustable Output CMOS Inverting Switching Regulators

MAX635/636/637

General Description

The MAX635/MAX636/MAX637 inverting switching regulators are designed for minimum component DC-DC conversion in the 5mW to 500mW range.

Low power applications require only a diode, output filter capacitor, and a low-cost inductor. An additional MOSFET and driver are needed for higher power applications. Low battery detection circuitry is included on chip.

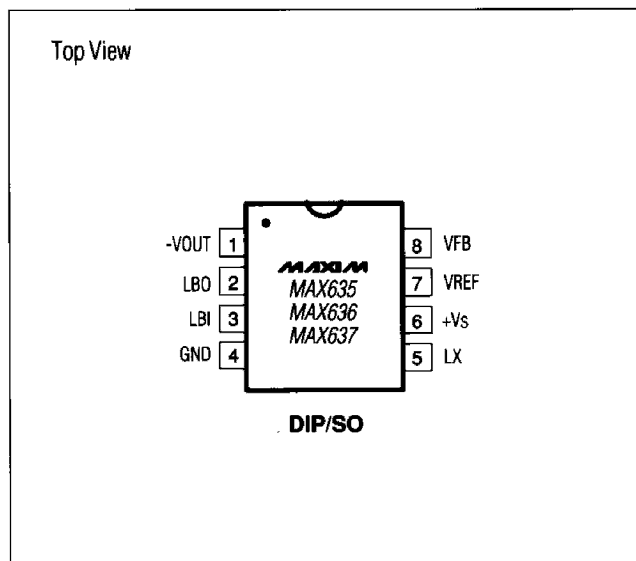
The MAX635/636/637 are preset for -5V, -12V, and -15V outputs, respectively. However, the regulators can be set to other levels by adding 2 resistors.

Maxim manufactures a broad line of step-up, step-down, and inverting DC-DC converters, with features such as logic-level shutdown, adjustable oscillator frequency, and external MOSFET drive.

Applications

- Minimum Component, High-Efficiency DC-DC Converters
- Portable Instruments
- Battery Power Conversion
- Board Level DC-DC Conversion

Pin Configuration



Features

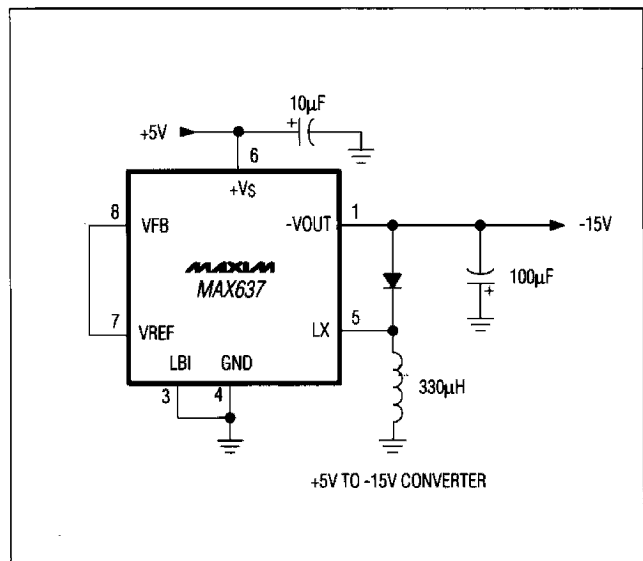
- ◆ Preset -5V, -12V, -15V Output Voltages
- ◆ Adjustable Output with 2 Resistors
- ◆ 85% Typ Efficiency
- ◆ Only 3 External Components
- ◆ 80 μ A Typ Operating Current
- ◆ Low Battery Detector

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX635XCPA	0°C to +70°C	8 Plastic DIP
MAX635XCSEA	0°C to +70°C	8 Narrow SO
MAX635XC/D	0°C to +70°C	Dice
MAX635XEPA	-40°C to +85°C	8 Plastic DIP
MAX635XESA	-40°C to +85°C	8 Narrow SO
MAX635XEJA	-40°C to +85°C	8 CERDIP
MAX635XMJA	-55°C to +125°C	8 CERDIP
MAX636XCPA	0°C to +70°C	8 Plastic DIP
MAX636XCSEA	0°C to +70°C	8 Narrow SO
MAX636XC/D	0°C to +70°C	Dice
MAX636XEPA	-40°C to +85°C	8 Plastic DIP
MAX636XESA	-40°C to +85°C	8 Narrow SO
MAX636XEJA	-40°C to +85°C	8 CERDIP
MAX636XMJA	-55°C to +125°C	8 CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy. Ordering Information continued on last page.

Typical Operating Circuit



Preset/Adjustable Output CMOS Inverting Switching Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +Vs (Note 1)	+18V
Input Voltage, LBO, LBI, VFB	-0.3V to (+Vs + 0.3V)
LX Output Current	525mA Peak
LBO Output Current	50mA
Power Dissipation	
Plastic DIP (derate 8.33mW/°C above +50°C)	625mW
Small Outline (derate 6mW/°C above +50°C)	450mW
CERDIP (derate 8mW/°C above +50°C)	800mW

Operating Temperature Range	
MAX63_C	0°C to +70°C
MAX63_E	-40°C to +85°C
MAX63_M	-55°C to +125°C
Storage Temperature	-65°C to +160°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	+Vs	TA = +25°C Over Temperature	2.3 2.6		16.5 16.5	V
Supply Current	Is	No Load, LX Off, Over Temperature +Vs = +5V +Vs = +15V		80 260	150 500	μA
Reference Voltage	VREF	TA = +25°C Over Temperature	1.24 1.20	1.31	1.38 1.42	V
VOUT Voltage (Note 2)		No Load, VFB = VREF, +Vs = +5V Over Temperature				
		MAX635A } 5% Output Accuracy MAX636A } MAX637A }	-4.75 -11.4 -14.25	-5.0 -12.0 -15.0	-5.25 -12.6 -15.75	V
		MAX635B } 10% Output Accuracy MAX636B } MAX637B }	-4.5 -10.8 -13.5	-5.0 -12.0 -15.0	-5.5 -13.2 -16.5	V
Efficiency				85		%
Line Regulation (Note 2)		+5V < +Vs < +15V		0.5		%VOUT
Load Regulation (Note 2)		POUT = 0mW to 150mW		0.2		%VOUT
Oscillator Frequency	f0	+Vs = +5V MAX63_A MAX63_B	45 40	50 50	56 65	kHz
Oscillator Duty Cycle		+Vs = +5V	40	50	60	%
LX On Resistance	RON	Ix = 100mA, +Vs = +5V = +15V		9 4	16 8	Ω
LX Leakage Current	IXL	+Vs = +16.5V TA = +25°C Over Temperature		0.01	1.0 30	μA
VFB Input Bias Current	IFB			0.01	10	nA
Low Battery Threshold	VLBI			1.31		V
Low Battery Input Bias Current	ILBI			0.01	10	nA
Low Battery Output Current	ILBO	V2 = +0.4V, V3 = +1.1V TA = 25°C Over Temperature	0.5	1.0		mA
Low Battery Output Leakage Current	ILBOL	V2 = +16.5V, V3 = +1.4V		0.01	3.0	μA

Note 1: In addition to the Absolute Maximum Rating of +18V, the input voltage also must not exceed 24V - | -VOUT |.

Note 2: Guaranteed by correlation with DC pulse measurements.

Preset/Adjustable Output CMOS Inverting Switching Regulators

Series Resistance (ESR). With low-cost aluminum electrolytic capacitors, the ESR produced ripple is often larger than that caused by the change in charge. Consequently, high quality aluminum or tantalum filter capacitors will minimize output ripple, even if smaller capacitance values are used. Best results at reasonable cost are typically achieved with a high quality aluminum electrolytic, in the 100 μ F to 500 μ F range, in parallel with a 0.1 μ F ceramic capacitor.

Application Hints

Inductor Saturation

When using off-the-shelf inductors, make sure that their peak current rating is observed. When designing your own inductors, observe the core manufacturer's Ampere-turns on NI ratings. Failure to observe the peak current or NI ratings may lead to saturation of the inductor, especially in circuits with external boosting transistors. Inductor saturation leads to very high current levels through the power switching device causing excessive power dissipation, poor efficiency, and possible damage.

Test for saturation by applying the maximum load and the maximum input voltage while monitoring the inductor current with a current probe. The normal inductor current waveform is a sawtooth with a linear current ramp. Saturation creates a nonlinear current waveform with a very rapid increase in current once the inductor saturates.

Ordering Information (continued)

PART*	TEMP. RANGE	PIN - PACKAGE
MAX637XCPA	0°C to +70°C	8 Plastic DIP
MAX637XCSA	0°C to +70°C	8 Narrow SO
MAX637XCJA	0°C to +70°C	8 CERDIP
MAX637XC/D	0°C to +70°C	Dice
MAX637XEPA	-40°C to +85°C	8 Plastic DIP
MAX637XESA	-40°C to +85°C	8 Narrow SO
MAX637XEJA	-40°C to +85°C	8 CERDIP
MAX637XMJA	-55°C to +125°C	8 CERDIP

*X = A for 5% Output Accuracy, X = B for 10% Output Accuracy.

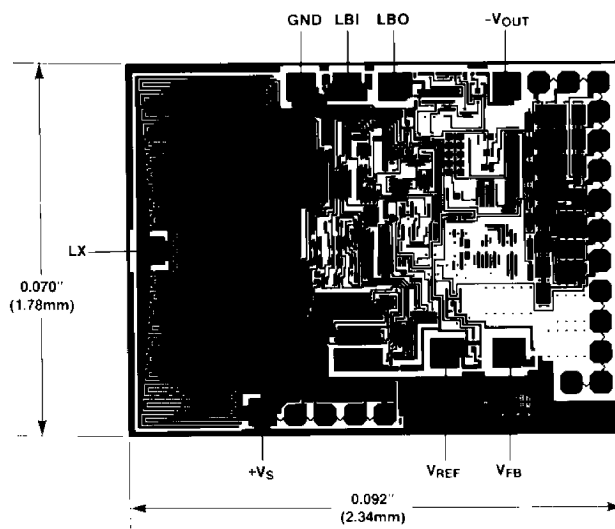
Bypassing and Compensation

The high current pulses in the LX output and the external inductor can cause erratic operation unless the MAX635/636/637 is properly bypassed. Connect a 10mF bypass capacitor directly across the device between +VS and GND to minimize the inductance and high frequency impedance of the power source. Also make sure that the high current ground return path of the inductor does not cause a voltage drop in the regulator's ground line.

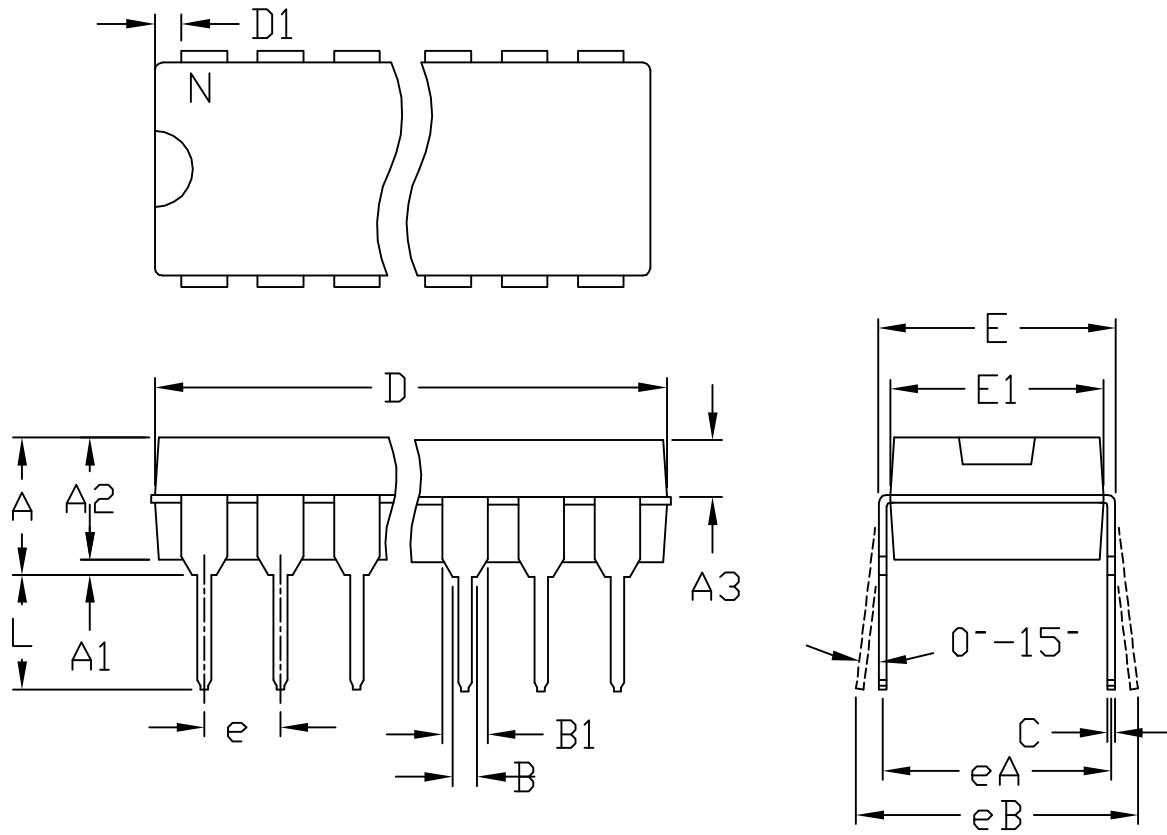
The reference voltage output, VREF, should be bypassed to ground with a 0.1 μ F capacitor. Avoid coupling to the high current path that includes the LX output and the inductor ground return.

When the value of the voltage setting resistors (R3 and R4, Figure 3) exceed 50k Ω , stray capacitance at the VFB input can add a "lag" to the feedback response causing output pulses to occur in bursts. This increases low-frequency ripple and lowers efficiency. This problem can often be avoided by minimizing lead lengths and circuit board trace size at the VFB node. Normal operation with evenly distributed output pulses can be restored by adding a "lead" compensation capacitor (100pF to 10nF) in parallel with R3.

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	BSC.	2.54	BSC.
eA	0.300	BSC.	7.62	BSC.
eB	0.400	BSC.	10.16	BSC.
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS		N	MS001
	MIN	MAX	MIN	MAX		
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

- NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
 5. SIMILIAR TO JEDEC MO-058AB
 6. N = NUMBER OF PINS