DC/DC Power Switching Regulator

The ISL8560 is a step down DC/DC power switching regulator which accepts 9.0V to 60V input and provides a 2A output current. The output voltage can be set in the range between 1.21V and 55V by means of an external divider. The device uses an internal power DMOS transistor with a typical $r_{DS(ON)}$ of 0.19Ω to obtain very high efficiency and high switching speed. A switching frequency in the range of 100kHz to 600kHz can be realized (the maximum power dissipation of the various packages must be observed). Notable features of this next generation of DC/DC converter includes pulse-by-pulse current limit for FET protection, hiccup mode for short circuit protection, voltage feedforward regulation, Frequency SYNC, soft-start, low standby current of 60µA typical in the disabled state, and thermal shut-down. The device is available in a 20 Ld QFN package.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8560IRZ	ISL 8560IRZ	-40 to +85	20 Ld 6x6 QFN	L20.6x6B
ISL8560IRZ-T*	ISL 8560IRZ	-40 to +85	20 Ld 6x6 QFN	L20.6x6B

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Voltage feedforward mode
- Step down DC/DC supporting up to 2A
- Input voltage range of 9.0V to 60V
- Internal reference of 1.21V ±1%
- Adjustable output voltage range of 1.21V to 55V
- Adjustable switching frequency 100kHz to 600kHz
- Frequency SYNC pin
- Zero load current operation
- Pulse-by-pulse mode current limit and Hiccup mode
- Low standby current of 60µA typical
- Thermal shut-down
- Load dump to 100V for 400ms
- Pb-Free (RoHS compliant)

Applications

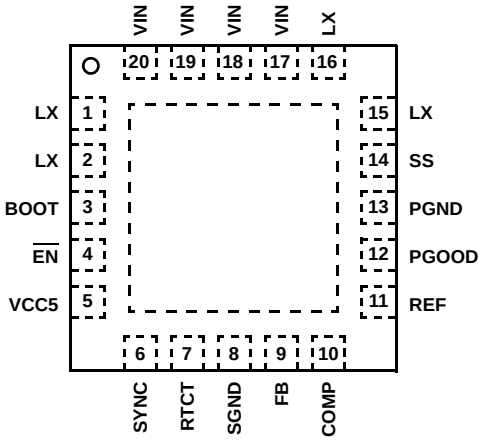
- Industrial and automotive power supplies
- Portable computers
- Battery chargers
- Distributed power systems

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Pinout

ISL8560
(20 LD QFN)
TOP VIEW



Absolute Maximum Ratings

Input Voltage VIN . . . . . GND - 0.3V to 72V
Voltage at BOOT pin . . . . . GND - 0.3V to 82V
LX, RTCT . . . . . GND - 0.3V to 60V
REF, FB, SS, $\overline{EN}$, SYNC, PGOOD pins 8V
VCC5* . . . . . GND - 0.3V to 5.5V

Recommended Operating Conditions

Junction Temperature Range . . . . . -40°C to +125°C
Supply Voltage Range (Typical) . . . . . 9.0V to 60V

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	30	1.5

Maximum Power Dissipation 3W
Maximum Junction Temperature (Hermetic Package or Die) . . +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**An accidental short between VCC5 and GND may cause excessive heating and permanent damage to the device.*

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Additional heatsinking may be required to insure that the junction temperature does not exceed above +125°C.

Electrical Specifications

Unless otherwise specified the specifications listed in the table are tested at T_A = +25°C and guard band for the full Temperature Range, V_{IN} = 48V, V_{OUT} = 5.0V, I_{OUT} = 0A. Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

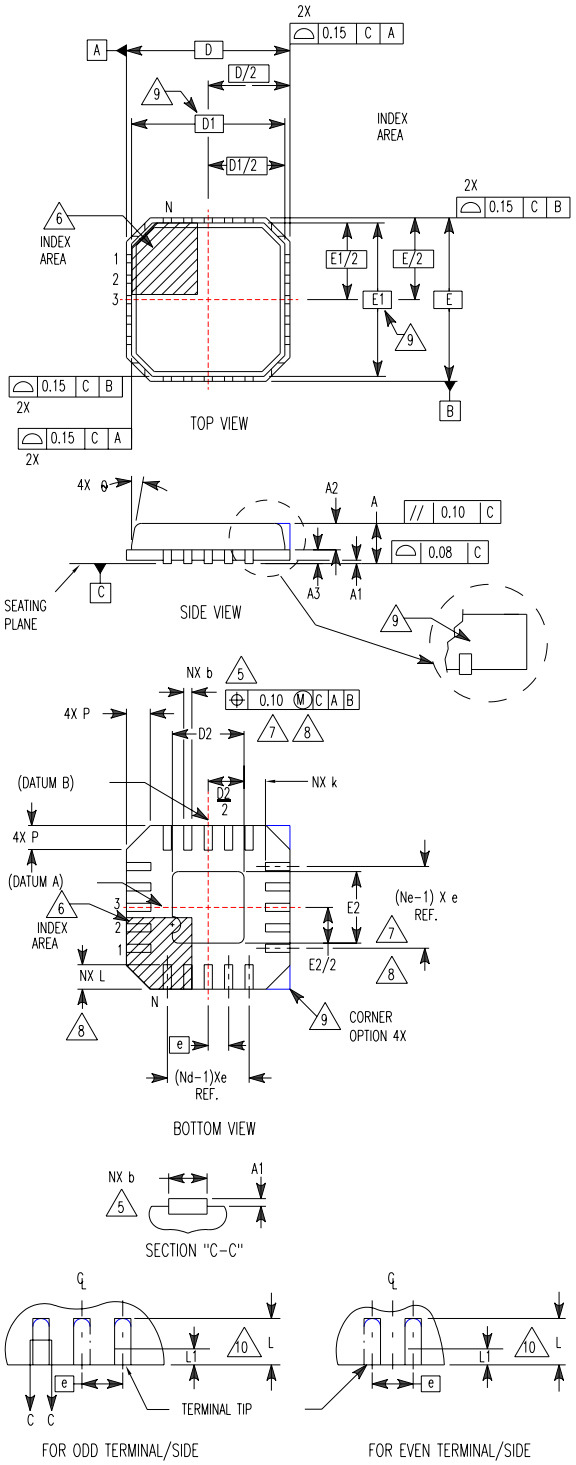
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN SUPPLY						
Input Voltage Range			9.0	24	60	V
VIN SUPPLY CURRENT						
Shut-down Current	IDD	V_{IN} = 9V, EN = HIGH		35	60	µA
		V_{IN} = 60V, EN = HIGH		60	110	µA
Operating Current	IDD	V_{IN} = 9V, V_{FB} = 1.5V		3.6	4	mA
		V_{IN} = 60V, V_{FB} = 1.5V		6.0	8.0	mA
VCC5 SUPPLY (A 1µF capacitor is needed from VCC5 to GND)						
VCC5 Output Voltage		V_{IN} = 9.0V to 60V, I_L = 0mA to 5mA	4.9	5.0	5.1	V
Maximum Output Current		V_{IN} = 24V			5	mA
INPUT UV						
Rising UV Threshold			7.8		8.9	V
UV Threshold Hysteresis			0.18	0.3	0.55	V
BUCK CONVERTER						
Output Voltage (Note 3)		I_{OUT} = 2A	1.2		V_{IN} - 5	V
Maximum Duty Cycle		F = 300kHz	90	96		%
Minimum Controllable ON Time		F = 300kHz		150		ns
OSCILLATOR						
Total Variation on Set Frequency		Over the V_{IN} range with frequency set by external resistor and capacitor at RTCT		±10		%
Frequency Range (Set by RTCT)	f_{OSC}		100		600	kHz
SYNC Range	f_{OSC}		100		600	kHz
Tested Oscillation Frequency	f_{OSC}	V_{IN} = 9V to 60V, R_T = 100kΩ, C_T = 1200pF		60		kHz
		V_{IN} = 9V to 60V, R_T = 27.4kΩ, C_T = 220pF		725		kHz

Electrical Specifications

Unless otherwise specified the specifications listed in the table are tested at T_A = +25°C and guard band for the full Temperature Range, V_{IN} = 48V, V_{OUT} = 5.0V, I_{OUT} = 0A. Typical values are at T_A = +25°C. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Max Ramp Amplitude	ΔV_{OSC}	V_{IN} = 9V		1		V_P
Modulator Gain	$V_{VIN}/\Delta V_{OSC}$			9		-
Min OFF Time				150	300	ns
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}			1.21		V
Soft-Start Current	I_{SS}		8	10	12	µA
Soft-Start Threshold	V_{SOFT}		0.8			V
ERROR AMPLIFIER						
Transconductance	g_m		3.9	5.7	7.2	mS
Gain-Bandwidth Product	GBW			15		MHz
Slew Rate	SR			6		V/µs
COMP Pin Drive	I_{COMP}			±200		µA
Internal Feedback Voltage	V_{FB}	T_A = -40°C to +85°C, V_{IN} = 9.0V to 60V	1.194	1.210	1.222	V
Internal Feedback Bias Current	I_{FB}	T_A = -40°C to +85°C, V_{FB} = 1.20V		±50	±100	nA
OVERCURRENT PROTECTION						
Dynamic Current Limit ON Time	t_{OCON}			16		Clock pulses
Dynamic Current Limit OFF Time	t_{OCOFF}			4		SS cycle
Switch Current Limit	I_{LIMIT}	T_A = +25°C	3.2	4.0	4.8	A
POWER-GOOD (OPEN DRAIN)						
Power-Good Lower Threshold	V_{PG-}	Fraction of the V_{OUT} set point; ~3µs noise filter	85		89	%
	V_{PG+}	Fraction of the V_{OUT} set point; ~3µs noise filter	111		115	%
PGOOD Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V			1	µA
PGOOD Voltage Low		I_{PGOOD} = 4mA			0.5	V
MOSFET						
Switch ON-Resistance	$r_{DS(ON)}$	I_{OUT} = 2A, V_{BOOT} = V_{IN} + 5.0V, Tested at wafer level		0.19	0.355	Ω
$\overline{EN}$						
Input HIGH Level (Asserted)	VINHIGH		2.6			V
Input LOW Level (Unasserted)	VINLOW				1.2	V
Input Current HIGH	I_{ENHIGH}	V_{IN} = 24V			25	µA
Input Current LOW	I_{ENLOW}	V_{IN} = 24V			25	µA
SYNC						
Input HIGH Level (Asserted)	VINHIGH		2.6			V
Input LOW Level (Unasserted)	VINLOW				1.2	V
Input Current HIGH	$I_{SYNCHIGH}$				0.2	µA
Input Current LOW	$I_{SYNCLOW}$				0.2	µA
THERMAL SHUT-DOWN						
Thermal Shut-down Temperature		Rising Threshold		150		°C
Thermal Shut-down Hysteresis				15		°C

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.6x6B

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJB ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.38	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.33	3.43	3.53	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.33	3.43	3.53	7, 8
e		0.80 BSC		-
k	0.635	-	-	-
L	0.50	0.60	0.70	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.