2.5A Synchronous Buck Regulator with Integrated MOSFETs

The ISL8502 is a synchronous buck controller with internal MOSFETs packaged in a small 4mmx4mm QFN package. The ISL8502 can support a continuous load of 2.5A and has a very wide input voltage range. With the switching MOSFETs integrated into the IC, the complete regulator footprint can be very small and provide a much more efficient solution than a linear regulator.

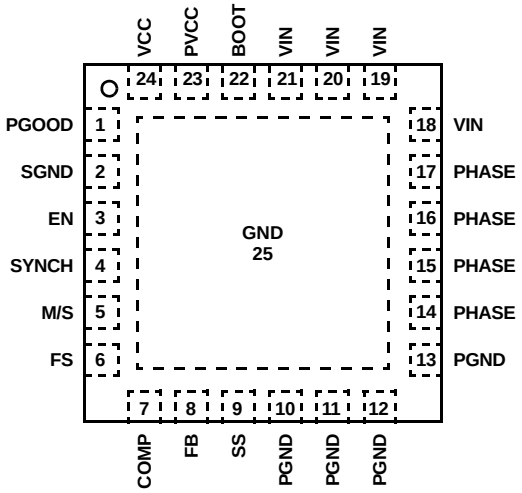
The ISL8502 is capable of stand alone operation or it can be used in a master slave combination for multiple outputs that are derived from the same input rail. Multiple slave channels (up to six) can be synchronized. This method minimizes the EMI and beat frequencies effect with multi-channel operation.

The switching PWM controller drives two internal N-Channel MOSFETs in a synchronous-rectified buck converter topology. The synchronous buck converter uses voltage-mode control with fast transient response. The switching regulator provides a maximum static regulation tolerance of ±1% over line, load, and temperature ranges. The output is user-adjustable by means of external resistors down to 0.6V.

The output is monitored for undervoltage events. The switching regulator also has overcurrent protection. Thermal shutdown is integrated. The ISL8502 features a bi-directional Enable pin that allows the part to pull the enable pin low during fault detection.

Pinout

ISL8502
(24 LD QFN)
TOP VIEW



Features

- Over 2.5A Continuous Output Current
- Integrated MOSFETs for Small Regulator Footprint
- Adjustable Switching Frequency, 500kHz to 1.2MHz
- Tight Output Voltage Regulation, ±1% Over-Temperature
- Wide Input Voltage Range, 5V ±10% or 5.5V to 14V
- Wide Output Voltage Range, from 0.6V
- Simple Single-Loop Voltage-Mode PWM Control Design
- Input Voltage Feed-Forward for Constant Modulator Gain
- Fast PWM Converter Transient Response
- Lossless $r_{DS(ON)}$ High Side and Low Side Overcurrent Protection
- Undervoltage Detection
- Integrated Thermal Shutdown Protection
- Power Good Indication
- Adjustable Soft-Start
- Start-Up with Pre-Bias Output
- Pb-Free (RoHS Compliant)

Applications

- Point of Load Applications
- Graphics Cards - GPU and Memory Supplies
- ASIC Power Supplies
- Embedded Processor and I/O supplies
- DSP Supplies

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL8502IRZ* (Note)	85 02IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4D

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

VIN . . . . . GND - 0.3V to +16.5V
VCC . . . . . GND - 0.3V to +6.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +22.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . +6.0V
All other Pins . . . . . GND - 0.3V to VCC + 0.3V

Recommended Operating Conditions

Supply Voltage on VIN . . . . . 5.5V to 14V
Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	39	2.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Minimum V_{IN} can operate below 5.5V as long as VCC is greater than 4.5V.
4. Maximum V_{IN} can be higher than 14V voltage stress across the upper and lower do not exceed 15.5V in all conditions.
5. Circuit requires 100ns minimum on time to detect overcurrent condition.
6. Limits established by characterization and are not production tested.

Electrical Specifications

Refer to Block and Simplified Power System Diagrams and Typical Application Schematics. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 5V ±10%, T_A = -40°C to +85°C. Typical are at T_A = +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} SUPPLY						
Input Voltage Range		V_{IN}	5.5[4]		14[5]	V
		V_{IN} tied to VCC	4.5		5.5	V
Input Operating Supply Current	I_Q	V_{FB} = 1.0V			7	mA
Input Standby Supply Current	I_{Q_SBY}	EN tied to GND, V_{IN} = 14V		1.25	2	mA
SERIES REGULATOR						
VCC Voltage	V_{PVCC}	V_{IN} > 5.6V	4.5	5.0	5.5	V
Maximum Output Current	I_{PVCC}	V_{IN} = 12V	50			mA
VCC Current Limit		V_{IN} = 12V, VCC shorted to PGND.		300		mA
POWER-ON RESET						
Rising VCC POR Threshold			4.2	4.4	4.49	V
Falling VCC POR Threshold			3.85	4.0	4.10	V
ENABLE						
Rising Enable Threshold Voltage	V_{EN_Rising}			2.7		V
Falling Enable Threshold Voltage	V_{EN_Fall}			2.3		V
Enable Sinking Current	I_{EN}				500	µA
OSCILLATOR						
PWM Frequency	f_{OSC}	R_T = 96kΩ	400	500	600	kHz
		R_T = 40kΩ	960	1200	1440	kHz
		FS pin tied to VCC		800		kHz
Ramp Amplitude	ΔV_{OSC}	V_{IN} = 14V		1.0		V
Ramp Amplitude	ΔV_{OSC}	V_{IN} = 5V		0.470		V

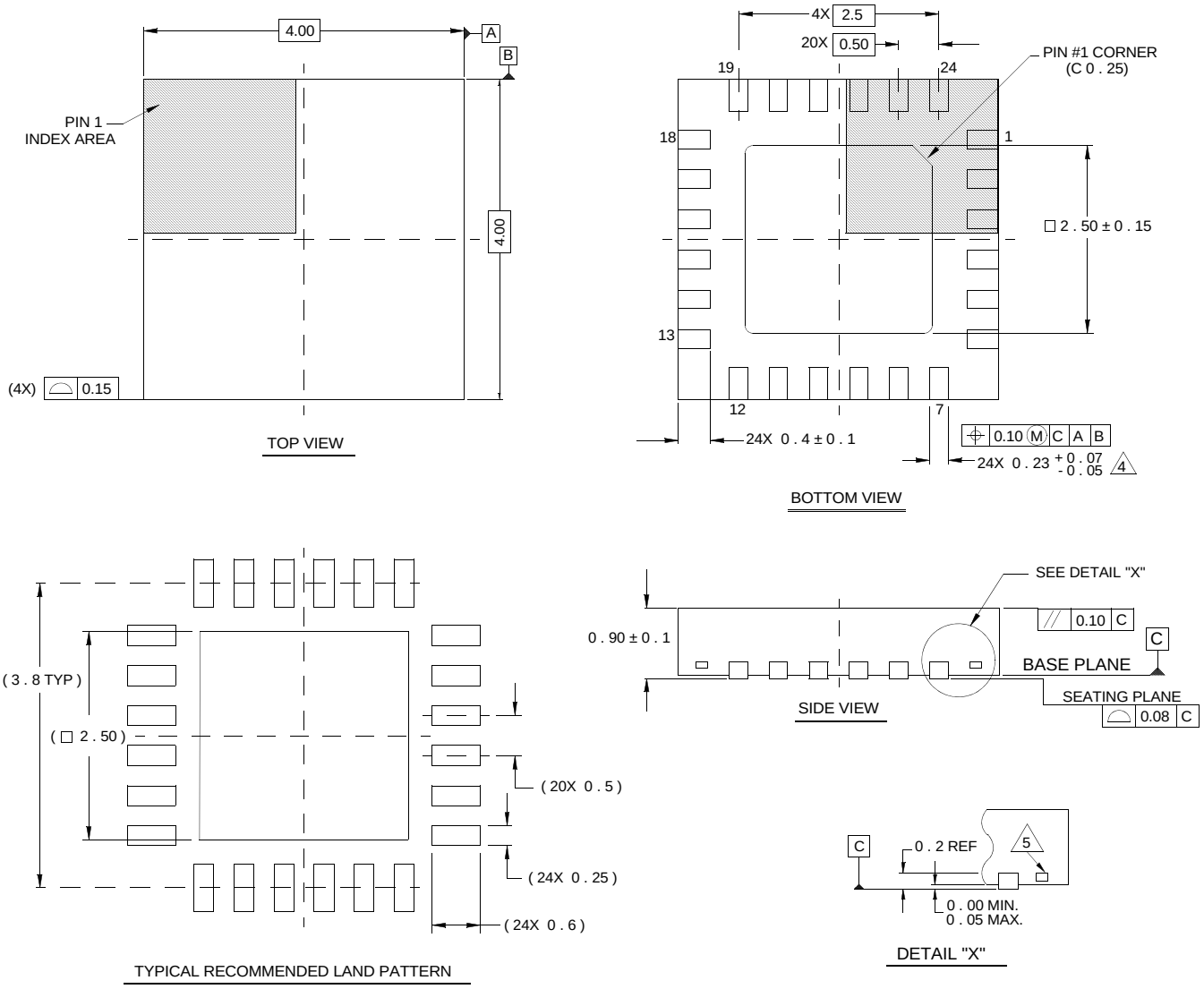
Electrical Specifications Refer to Block and Simplified Power System Diagrams and Typical Application Schematics. Operating Conditions Unless Otherwise Noted: V_{IN} = 12V, or V_{CC} = 5V ±10%, T_A = -40°C to +85°C. Typical are at T_A = +25°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Modulator Gain	$V_{VIN}/\Delta V_{OSC}$	By Design		8		-
Maximum Duty Cycle	D_{MAX}	f_{OSC} = 500kHz	88			%
Maximum Duty Cycle	D_{MAX}	f_{OSC} = 1.2MHz	76			%
REFERENCE VOLTAGE						
Reference Voltage	V_{REF}			0.600		V
System Accuracy			-1.0		+1.0	%
FB Pin Bias Current				±80	±200	nA
SOFT-START						
Soft-Start Current	I_{SS}		20	30	40	µA
Enable Soft-Start Threshold			0.8	1.0	1.2	V
Enable Soft-Start Threshold Hysteresis				12		mV
Enable Soft-Start Voltage High			2.8	3.2	3.8	V
ERROR AMPLIFIER						
DC Gain				88		dB
Gain-Bandwidth Product	GBWP			15		MHz
Maximum Output Voltage			3.9	4.4		V
Slew Rate	SR			5		V/µs
INTERNAL MOSFETS						
Upper MOSFET $r_{DS(ON)}$	r_{DS_Upper}	V_{CC} = 5V		180		mΩ
Lower MOSFET $r_{DS(ON)}$	r_{DS_Lower}	V_{CC} = 5V		90		mΩ
PGOOD						
PGOOD Threshold	V_{FB}/V_{REF}	Rising Edge Hysteresis 1%	107	111	115	%
		Falling Edge Hysteresis 1%	86	90	93	%
PGOOD Rising Delay	t_{PGOOD_DELAY}	f_{OSC} = 500kHz		250		ms
PGOOD Leakage Current		V_{PGOOD} = 5.5V			5	µA
PGOOD Low Voltage	V_{PGOOD}			0.10		V
PGOOD Sinking Current	I_{PGOOD}				0.5	mA
PROTECTION						
Positive Current Limit	I_{POC}	V_{IN} = V_{CC} = 5V, IOC from PHASE to PGND. (Notes 5, 6)	2.8	3.5	4.0	A
Negative Current Limit	I_{NOC}	V_{IN} = V_{CC} = 5V, IOC from VIN to PHASE. (Notes 5, 6)	2.2	3.0	3.5	A
Undervoltage Level	V_{FB}/V_{REF}		76	80	84	%
Thermal Shutdown Setpoint	T_{SD}			150		°C
Thermal Recovery Setpoint	T_{SR}			130		°C

Package Outline Drawing

L24.4x4D

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.