DS2404
EconoRAM Time Chip

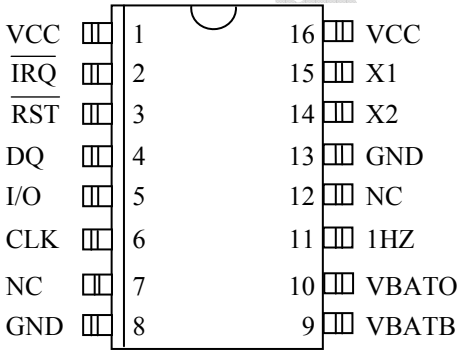
FEATURES

- 4096 bits of nonvolatile dual-port memory including real time clock/calendar in binary format, programmable interval timer, and programmable power-on cycle counter
- 1-Wire® interface for MicroLAN communication at 16.3kbits/s
- 3-wire host interface for high-speed data communications at 2Mb/s
- Unique, factory-lasered and tested 64-bit registration number (8-bit family code + 48-bit serial number + 8-bit CRC tester) assures absolute traceability because no two parts are alike
- Memory partitioned into 16 pages of 256-bits for packetizing data
- 256-bit scratchpad with strict read/write protocols ensures integrity of data transfer
- Programmable alarms can be set to generate interrupts for interval timer, real time clock, and/or cycle counter
- 16-pin DIP, SO, and SSOP packages
- Operating temperature range from -40°C to +85°C
- Operating voltage range from 2.8V to 5.5V

ORDERING INFORMATION

DS2404-001	16-pin DIP
DS2404S-001	16-pin SO
DS2404B	16-pin SSOP
DS2404S-001/T&R	Tape and Reel of S2404S-001
DS2404B/T&R	Tape and Reel of DS2404B

PIN ASSIGNMENT



16-PIN DIP (300 MIL)
16-PIN SO (300 MIL)
16-PIN SSOP (208 MIL)
See Mechanical Drawings Section

PIN DESCRIPTION

V_{CC}	– 2.8 to 5.5V
$\overline{IRQ}$	– Interrupt Output
$\overline{RST}$	– 3-Wire Reset Input
DQ	– 3-Wire Input/Output
I/O	– 1-Wire Input/Output
CLK	– 3-Wire Clock Input
NC	– No Connection
GND	– Ground
V_{BATB}	– Battery Backup Input
V_{BATO}	– Battery Operate Input
1Hz	– 1Hz Output
X_1, X2	– Crystal Connections

DESCRIPTION

The DS2404 EconoRAM Time Chip offers a simple solution for storing and retrieving vital data and time information with minimal hardware. The DS2404 contains a unique lasered ROM, real-time clock/calendar, interval timer, cycle counter, programmable interrupts, and 4096-bits of SRAM. Two separate ports are provided for communication: 1-Wire and 3-wire. Using the 1-Wire port, only one pin is required for communication, and the lasered-ROM can be read even when the DS2404 is without power. The 3-wire port provides high-speed communication using the traditional Dallas Semiconductor 3-wire interface. With either interface, a strict protocol for accessing the DS2404 ensures data integrity. Utilizing backup energy sources, the data is nonvolatile (NV) and allows for stand-alone operation.

1-Wire is a registered trademark of Dallas Semiconductor.

ABSOLUTE MAXIMUM RATINGS*

Voltage on DATA to Ground	-0.5V to +7.0V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED OPERATING CONDITIONS (-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH3}	2.2		V_{CC} +0.3	V	1
Logic 0	V_{IL3}	-0.3		+0.8	V	1
$\overline{RST}$ Logic 1		2.8		5.5	V	1
Supply	V_{CC}	2.8		5.5	V	1
Battery	V_{BATB}, V_{BATO}	2.8	3.0	5.5	V	1,6

DC ELECTRICAL CHARACTERISTICS (1-WIRE PORT) (-40°C to +85°C; V_{CC} = 5V+ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH1}	2.2		6.0	V	1,9
Logic 0	V_{IL1}	-0.3		+0.8	V	1,16
Output Logic Low @ 4mA	V_{OL}			0.4	V	1
Output Logic High	V_{OH}			V_{PUP}	V	1,12
Input Load Current	I_L		5		µA	13

DC ELECTRICAL CHARACTERISTICS (V_{CC} OP. MODE) (-40°C to +85°C; V_{CC} = 5V+ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	I_{LO}			1	µA	17
Output Current @ 2.4V on DQ	I_{OH}	3			mA	18
Output Current @ 0.4V on DQ	I_{OL}			-3	mA	19
Active Current	I_{CC1}			2	mA	5
Standby Current	I_{CC2}			500	µA	11

DC ELECTRICAL CHARACTERISTICS (BATT. OP. MODE) (-40°C to +85°C; V_{BATO} = 3.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Output Leakage	I_{LO}			1	µA	17
Output Current @ 2.4V on DQ	I_{OH}	1			mA	18
Output Current @ 0.4V on DQ	I_{OL}			-1	mA	19
I/O Operate Charge	Q_{BATO}			200	nC	10
Battery Current (OSC On)	I_{BAT1}			350	nA	7
Battery Current (OSC Off)	I_{BAT2}			200	nA	7,21

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			15	pF	
I/O (1-Wire)	$I_{IN/OUT}$		100	800	pF	8

RESISTANCES

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{RST}$ Resistance to Ground	Z_{RST}		65		kΩ	
DQ Resistance to Ground	Z_{DQ}		65		kΩ	
CLK Resistance to Ground	Z_{CLK}		65		kΩ	

AC ELECTRICAL CHARACTERISTICS: 3-WIRE PORT

(-40°C to +85°C; V_{CC} = 5V+ 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	35			ns	2
CLK to Data Hold	t_{CDH}	40			ns	2
CLK to Data Delay	t_{CDD}			100	ns	2,3,4
CLK Low Time	t_{CL}	250			ns	2
CLK High Time	t_{CH}	250			ns	2
CLK Frequency	t_{CLK}	DC		2.0	MHz	2
CLK Rise and Fall	t_R,t_F			500	ns	2
$\overline{RST}$ to CLK Setup	t_{CC}	1			µs	2
CLK to $\overline{RST}$ Hold	t_{CCH}	40			ns	2
$\overline{RST}$ Inactive Time	t_{CWH}	250			ns	2
CLK or $\overline{RST}$ to DQ High Z	t_{CDZ}			50	ns	2

AC ELECTRICAL CHARACTERISTICS: 1-WIRE PORT

(-40°C to +85°C; V_{CC} =2.8 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}	60		120	µs	
Write 1 Low Time	t_{LOW1}	1		15	µs	23
Write 0 Low Time	t_{LOW0}	60		120	µs	
Read Low Time	t_{LOWR}	1		15	µs	23
Read Data Valid	t_{RDV}		15		µs	22
Release Time	$t_{RELEASE}$	0	15	45	µs	
Read Data Setup	t_{SU}			1	µs	15
Recovery Time	t_{REC}	1			µs	
Interrupt	t_{INT}	960		4800	µs	
Reset Time High	t_{RSTH}	480			µs	14
Reset Time Low	t_{RSTL}	480		960	µs	20
Presence Detect High	t_{PDH}	15		60	µs	
Presence Detect Low	t_{PDL}	60		240	µs	

NOTES:

1. All voltages are referenced to ground.
2. V_{IH} = 2.0V or V_{IL} = 0.8V with 10ns maximum rise and fall time.
3. V_{DQH} = 2.4V and V_{DQL} = 0.4V, respectively.
4. Load capacitance = 50pF.
5. Measured with outputs open.
6. When battery is applied to V_{BATO} input, V_{CC} and V_{BATB} must be 0V.
7. $V_{BATB,}$ or V_{BATO} = 3.0V; all inputs inactive state.
8. Capacitance on the I/O pin could be 800pF when power is first applied. If a 5kΩ resistor is used to pull-up the I/O line to $V_{PUP,}$ 5µs after power has been applied, the parasite capacitance will not affect normal communications.
9. For auto-mode operation of the interval timer, the high level on the I/O pin must be greater than or equal to 70% of V_{CC} or $V_{BATO.}$
10. Read and write scratchpad (all 32 bytes) at 3.0V.
11. All other inputs at CMOS levels.
12. V_{PUP} = external pull-up voltage.
13. Input load is to ground.
14. An additional reset or communication sequence cannot begin until the reset high time has expired.
15. Read data setup time refers to the time the host must pull the I/O line low to read a bit. Data is guaranteed to be valid within 1µs of this falling edge.
16. Under certain low voltage conditions V_{IL1MAX} may have to be reduced to as much as 0.5V to always guarantee a presence pulse.
17. Applies to 1 Hz and $\overline{IRQ}$ pins only.
18. Applies to DQ pin only.
19. Applies to DQ, 1Hz and $\overline{IRQ}$ pins only.

20. The reset low time (t_{RSTL}) should be restricted to a maximum of 960µs, to allow interrupt signaling, otherwise, it could mask or conceal interrupt pulses.

21. When the battery is attached, the oscillator powers up in the off state.

22. The optimal sampling point for the master is as close as possible to the end time of the 15µs t_{RDV} period without exceeding t_{RDV}. For the case of a Read-one time slot, this maximizes the amount of time for the pull-up resistor to recover the line to a high level. For a Read-zero time slot it ensures that a read will occur before the fastest 1-Wire device(s) release the line ($t_{RELEASE} = 0$).

23. The duration of the low pulse sent by the master should be a minimum of 1µs with a minimum value as short as possible to allow time for the pull-up resistor to recover the line to a high level before the 1-Wire device samples in the case of a Write 1 Low Time or before the master samples in the case of a Read Low Time.