8V to 14V, Single-Phase Synchronous Buck Pulse-Width Modulation (PWM) Controller With Integrated Gate Drivers

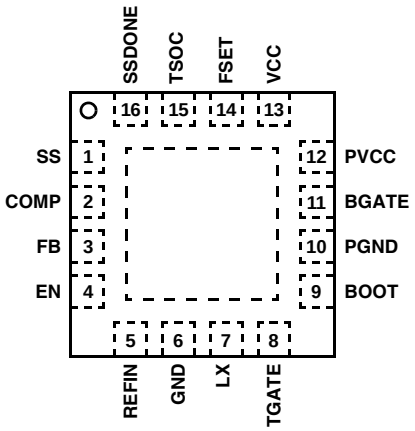
The ISL8104 is a 8V to 14V synchronous PWM controller with integrated MOSFET drivers. The controller features the ability to safely start-up into prebiased output loads and provides protection against overcurrent fault events. Overcurrent protection is implemented using top-side MOSFET $r_{DS(ON)}$ sensing, eliminating the need for a current sensing resistor.

The ISL8104 employs voltage-mode control with dual-edge modulation to achieve fast transient response. The operating frequency is adjustable from 50kHz to 1.5MHz with full (0% to 100%) PWM duty cycle capability. The error amplifier features a 15MHz (typ) gain-bandwidth product and 6V/µs slew rate enabling high converter bandwidth.

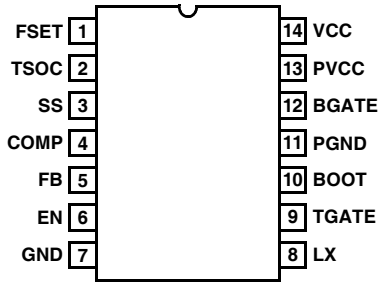
The output voltage of the converter can be regulated to as low as 0.597V with a tolerance of ±1.0% over the commercial temperature range (0°C to +70°C), and ±1.5% over industrial temperature range (-40°C to +85°C). Provided in the QFN package, a SS pin and REFIN pin enable supply sequencing and voltage tracking functionality.

Pinouts

ISL8104 (16 LD QFN)
TOP VIEW



ISL8104 (14 LD SOIC)
TOP VIEW



Features

- +8V ±5% to +14V ±10% Bias Voltage Range
  - 1.5V to 15.4V Input Voltage Range
- 0.597V Internal Reference Voltage
  - ±1.0% Over the Commercial Temperature Range
  - ±1.5% Over the Industrial Temperature Range
- Voltage-Mode PWM Control with Dual-Edge Modulation
- 14V High Speed N-Channel MOSFET Gate Drivers
  - 2.0A Source/3A Sink at 14V Bottom-Side Gate Drive
  - 1.25A Source/2A Sink at 14V Top-Side Gate Drive
- Fast Transient Response
  - 15MHz (typ) Gain-Bandwidth Error Amplifier with 6V/µs slew rate
  - Full 0% to 100% Duty Cycle Support
- Programmable Operating Frequency from 50kHz to 1.5MHz
- Lossless Programmable Overcurrent Protection
  - Top-Side MOSFET's $r_{DS(ON)}$ Sensing
  - ~120ns Blanking Time
- Sourcing and Sinking Current Capability
- Support for Start-Up into Prebiased Loads
- Soft-Start Done and an External Reference Pin for Tracking Applications are Available in the QFN Package
- Pb-free available (RoHS compliant)

Applications

- Test and Measurement Instruments
- Distributed DC/DC Power Architecture
- Industrial Applications
- Telecom/Datacom Applications

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8104CBZ*	8104CBZ	0 to +70	14 Ld SOIC	M14.15
ISL8104IBZ*	8104IBZ	-40 to +85	14 Ld SOIC	M14.15
ISL8104CRZ*	81 04CRZ	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL8104IRZ*	81 04IRZ	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL8104EVAL1Z	Evaluation Board			
ISL8104EVAL2Z	Evaluation Board			

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage, V_{PVCC}, V_{VCC} . . . . . GND - 0.3V to +16V
Enable Voltage, V_{EN} . . . . . GND - 0.3V to +16V
Soft-start Done Voltage, V_{SSDONE} . . . . . GND - 0.3V to +16V
TSOC Voltage, V_{TSOC} . . . . . GND - 0.3V to +16V
BOOT Voltage, V_{BOOT} . . . . . GND - 0.3V to +36V
LX Voltage, V_{LX} . . . . . V_{BOOT} - 16V to V_{BOOT} + 0.3V
All Other Pins . . . . . GND - 0.3V to 5.0V
ESD Rating
ESD Classification . . . . . Class 2

Operating Conditions

Supply Voltage, V_{VCC} . . . . . +8V ±5% to +14V ±10%
Supply Voltage, V_{PVCC} . . . . . +8V ±5% to +14V ±10%
Boot to Phase Voltage, V_{BOOT} - V_{LX} . . . . . $<V_{PVCC}$
Ambient Temperature Range, ISL8104C . . . . . 0°C to +70°C
Ambient Temperature Range, ISL8104I . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	95	N/A
QFN Package (Notes 2, 3)	47	8.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. Limits should be considered typical and are not production tested.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted, specifications in **bold** are valid for process, temperature, and line operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} SUPPLY CURRENT						
Shutdown Supply V_{CC}	I_{VCC}	SS/EN = 0V	3.5	6.1	8.5	mA
Shutdown Supply V_{PVCC}	I_{PVCC}	SS/EN = 0V	0.30	0.5	0.75	mA
POWER-ON RESET						
V_{CC}/V_{PVCC} Rising Threshold			6.45	7.10	7.55	V
V_{CC}/V_{PVCC} Hysteresis			170	250	500	mV
TSOC Rising Threshold			0.70	0.73	0.75	V
TSOC Hysteresis			180	200	220	mV
Enable - Rising Threshold			1.4	1.5	1.60	V
Enable - Hysteresis			175	250	325	mV
REFERENCE						
Reference Voltage		T_J = 0°C to +70°C	0.591	0.597	0.603	V
		T_J = -40°C to +85°C	0.588	0.597	0.606	V
System Accuracy		T_J = 0°C to +70°C	-1.0	-	1.0	%
		T_J = -40°C to +85°C	-1.5	-	1.5	%
REFIN Current Source (QFN Only)			-4	-6	-8	µA
REFIN Threshold (QFN Only)			2.10	-	3.50	V
REFIN Offset (QFN Only)			-3	-	3	mV

Electrical Specifications Recommended Operating Conditions, unless otherwise noted, specifications in **bold** are valid for process, temperature, and line operating conditions. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Trim Test Frequency		R_{FSET} = OPEN V_{VCC} = 12	175	200	220	kHz
Total Variation (Note 4)		8kΩ < R_{FSET} to GND < 200kΩ	-	±15	-	%
Ramp Amplitude	ΔV_{OSC}	R_{FSET} = OPEN	1.7	1.9	2.15	V_{P-P}
Ramp Bottom (Note 4)			-	1	-	V
ERROR AMPLIFIER						
DC Gain (Note 4)		R_L = 10kΩ, C_L= 100pF	-	88	-	dB
Gain-Bandwidth Product (Note 4)	GBWP	R_L = 10kΩ, C_L= 100pF	-	15	-	MHz
Slew Rate (Note 4)	SR	R_L = 10kΩ, C_L= 100pF	-	6	-	V/µs
COMP Source Current (Note 4)	$I_{COMPSRC}$		-	2	-	mA
COMP Sink Current (Note 4)	$I_{COMPSNK}$		-	2	-	mA
GATE DRIVERS						
Top-side Drive Source Current (Note 4)	I_{T_SOURCE}	V_{BOOT} - V_{LX} = 14V, 3nF Load	-	1.25	-	A
Top-side Drive Source Impedance	R_{T_SOURCE}	90mA Source Current	-	2.0	-	Ω
Top-side Drive Sink Current (Note 4)	I_{T_SINK}	V_{BOOT} - V_{LX} = 14V, 3nF Load	-	2	-	A
Top-side Drive Sink Impedance	R_{T_SINK}	90mA Source Current	-	1.3	-	Ω
Bottom-side Drive Source Current (Note 4)	I_{B_SOURCE}	V_{PVCC} = 14V, 3nF Load	-	2	-	A
Bottom-side Drive Source Impedance	R_{B_SOURCE}	90mA Source Current	-	1.3	-	Ω
Bottom-side Drive Sink Current (Note 4)	I_{B_SINK}	V_{PVCC} = 14V, 3nF Load	-	3	-	A
Bottom-side Drive Sink Impedance	R_{B_SINK}	90mA Source Current	-	0.94	-	Ω
PROTECTION						
TSOC Current	I_{TSOC}	T_J = 0°C to +70°C	180	200	220	µA
		T_J = -40°C to +85°C	176	200	224	µA
TSOC Measurement Offset (Note 4)	OCP_{OFFSET}	TSOC = 1.5V to 15.4V	-	±10	-	mV
SOFT-START						
Soft-start Current	I_{SS}		22	30	38	µA
SSDONE Low Output Voltage (QFN ONLY)		I_{SSDONE} = 2mA	-	-	0.30	V

Functional Pin Description (QFN/SOIC)

SS (Pin 1/3)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 30µA current source, sets the soft-start interval of the converter.

COMP (Pin 2/4) and FB (Pin 3/5)

COMP and FB are the available external pins of the error amplifier. The FB pin is the inverting input of the error amplifier and the COMP pin is the error amplifier output. These pins are used to compensate the voltage-control feedback loop of the converter.

EN (Pin 4/6)

This pin is a TTL compatible input. Pull this pin below 0.8V to disable the converter. In shutdown the soft-start pin is discharged and the TGATE and BGATE pins are held low.

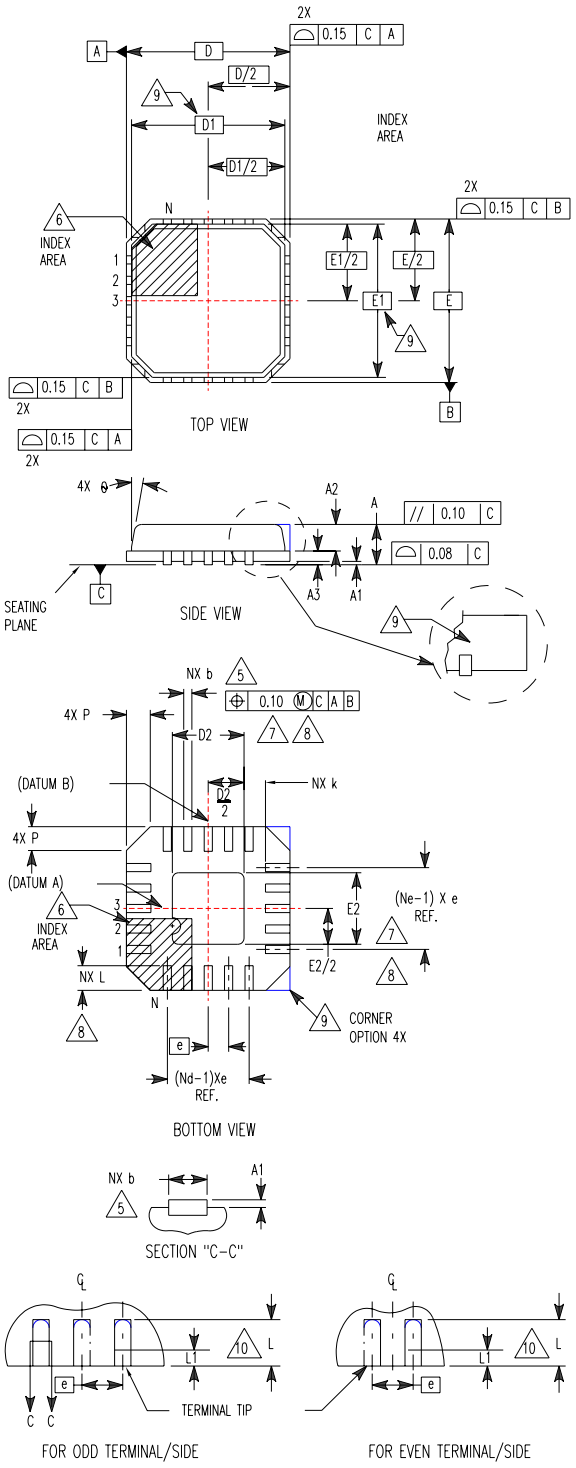
REFIN (QFN ONLY Pin 5)

Upon enable if REFIN is less than 2.2V, the external reference pin is used as the control reference instead of the internal 0.597V reference. An internal 6µA pull-up to 5V is provided for disabling this functionality.

GND (Pin 6/7)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

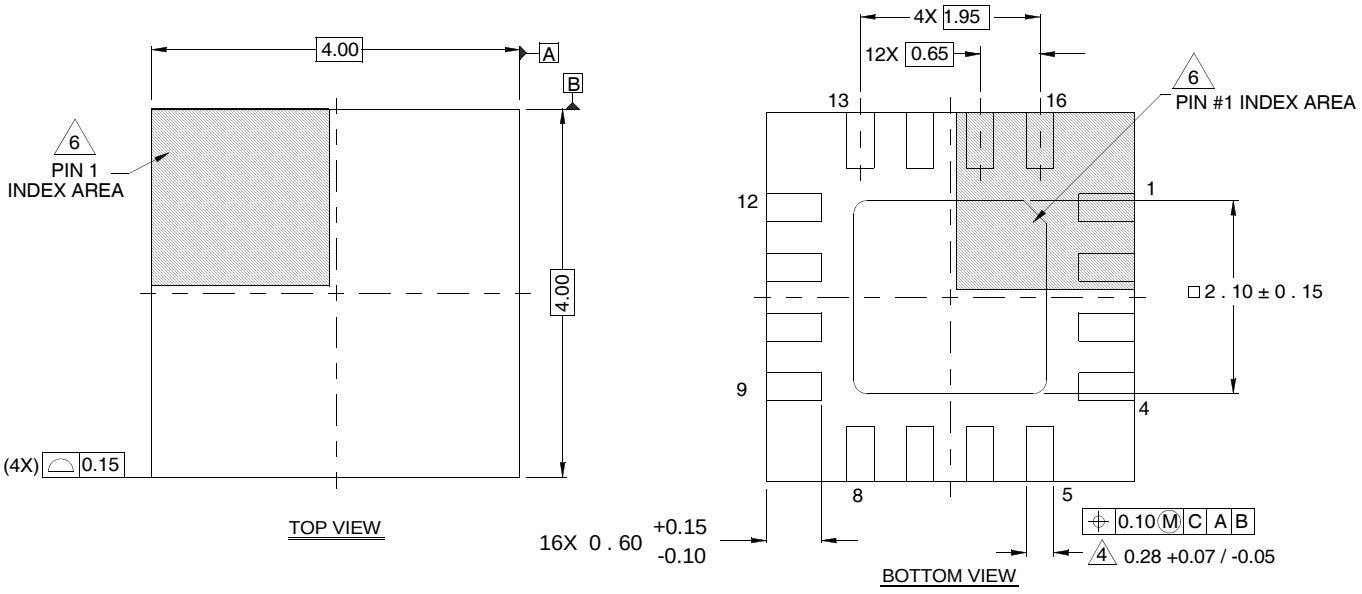
NOTES:

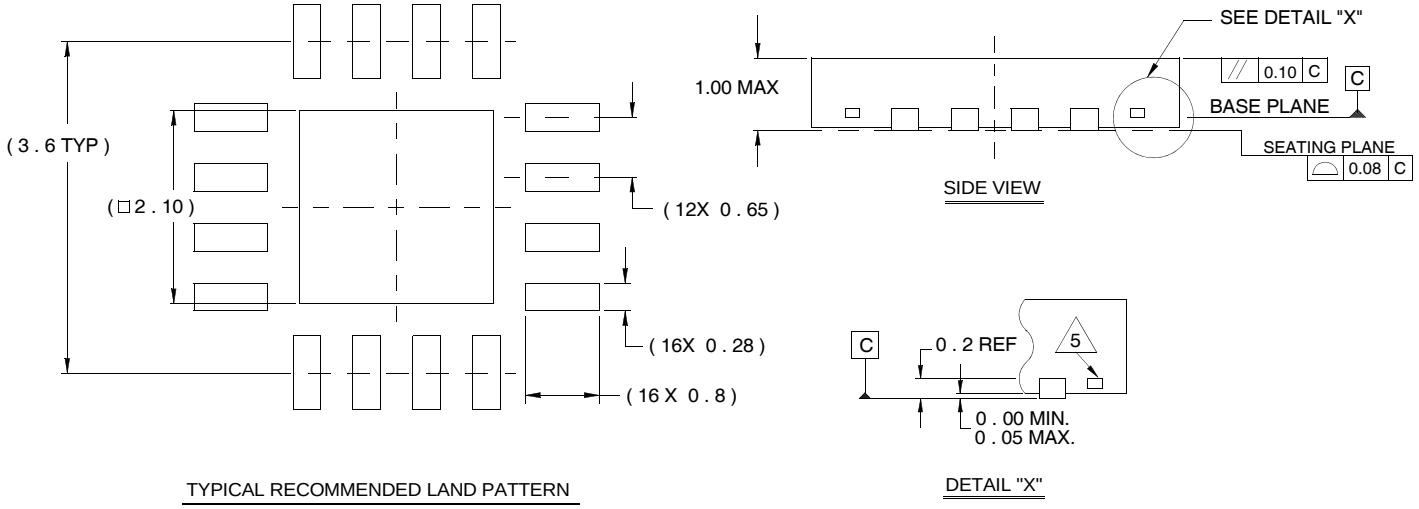
1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Package Outline Drawing

L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.