Data Sheet June 6, 2005 FN9144.4

Wide Input Range Dual PWM Controller with DDR Option

The ISL6539 dual PWM controller delivers high efficiency and tight regulation from two voltage regulating synchronous buck DC/DC converters. It was designed especially for DDR DRAM, SDRAM, graphic chipset applications, and system regulators in high performance applications.

Voltage-feed-forward ramp modulation, current mode control, and internal feedback compensation provide fast response to input voltage and output load transients. Input current ripple is minimized by channel-to-channel PWM phase shift of 0°, 90°, or 180° (determined by input voltage and status of the DDR pin).

The ISL6539 can control two independent output voltages adjustable from 0.9V to 5.5V or, by activating the DDR pin, transform into a complete DDR memory power supply solution. In DDR mode, CH2 output voltage VTT tracks CH1 output voltage VDDQ. CH2 output can both source and sink current, an essential power supply feature for DDR memory. The reference voltage VREF required by DDR memory is generated as well.

In dual power supply applications the ISL6539 monitors the output voltage of both CH1 and CH2. An independent PGOOD (power good) signal is asserted for each channel after the soft-start sequence has completed, and the output voltage is within PGOOD window. In DDR mode CH1 generates the only PGOOD signal.

Built-in overvoltage protection prevents the output from going above 115% of the set point by holding the lower MOSFET on and the upper MOSFET off. When the output voltage decays below the overvoltage threshold, normal operation automatically resumes. Once the soft-start sequence has completed, undervoltage protection latches the offending channel off if the output drops below 75% of its set point value for the dual switcher. Adjustable overcurrent protection (OCP) monitors the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET. If more precise current-sensing is required, an external current sense resistor may be used.

Features

- Provides regulated output voltage in the range 0.9V-5.5V
- Complete DDR memory power solution with VTT tracks VDDQ/2 and VDDQ/2 buffered reference output
- Supports both DDR-I and DDR2 memory
- Lossless $r_{DS(ON)}$ current-sense sensing
- Excellent dynamic response with voltage feed-forward and current mode control accommodating wide range LC filter selections
- Dual mode operation–operates directly from a 5.0-15V input or 3.3V/5V system rail
- Undervoltage lock-out on VCC pin
- Power-good, overcurrent, overvoltage, undervoltage protection for both channels
- Synchronized 300kHz PWM operation in PWM mode
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Single and Dual Channel DDR Memory Power Systems
- Graphics cards - GPU and memory supplies
- Supplies for Servers, Motherboards, FPGAs
- ASIC power supplies
- Embedded processor and I/O supplies
- DSP supplies

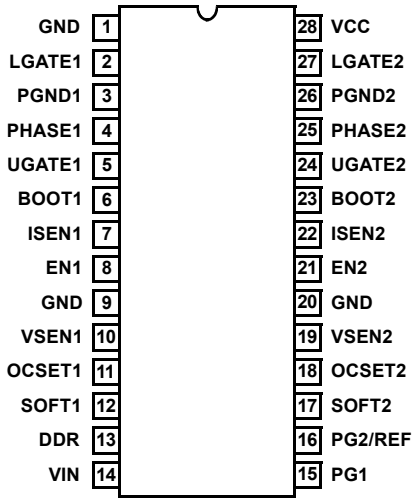
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6539CA	0 to 70	28 Ld SSOP	M28.15
ISL6539CA-T	28 Ld SSOP Tape and Reel		
ISL6539CAZ (Note)	0 to 70	28 Ld SSOP (Pb-Free)	M28.15
ISL6539CAZ-T (Note)	28 Ld SSOP Tape and Reel (Pb-Free)		
ISL6539IA	-40 to 85	28 Ld SSOP	M28.15
ISL6539IA-T	28 Ld SSOP Tape and Reel		
ISL6539IAZ (Note)	-40 to 85	28 Ld SSOP (Pb-Free)	M28.15
ISL6539IAZ-T (Note)	28 Ld SSOP Tape and Reel (Pb-Free)		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL6539 (SSOP)
TOP VIEW



Absolute Maximum Ratings

Bias Voltage, V_{CC} . . . . . +6.5V
Input Voltage, V_{IN} . . . . . +18.0V
PHASE, UGATE . . . . . GND-5V (Note 1) to +24.0V
BOOT, ISEN . . . . . GND-0.3V to +24.0V
BOOT with respect to PHASE . . . . . + 6.5V
All Other Pins . . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Bias Voltage, V_{CC} . . . . . +5.0V ±5%
Input Voltage, V_{IN} . . . . . +3.3V or 5.0V to +18.0V
Ambient Temperature Range, Commercial . . . . . 0°C to 70°C
Junction Temperature Range, Commercial . . . . . 0°C to 125°C
Ambient Temperature Range, Industrial. . . . . -40°C to 85°C
Junction Temperature Range, Industrial . . . . . -40°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SSOP Package	80

Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. 250ns transient. See Confining The Negative Phase Node Voltage Swing in Application Information Section.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Bias Current	I_{CC}	LGATEx, UGATEx Open, VSENx forced above regulation point, DDR = 0, VIN > 5V	-	1.8	3.0	mA
Shut-down Current	I_{CCSN}		-	-	1	µA
VCC UVLO						
Rising VCC Threshold	V_{CCU}		4.30	4.45	4.50	V
Falling VCC Threshold	V_{CCD}		4.00	4.14	4.34	V
VIN						
Input Voltage Pin Current (Sink)	I_{VIN}		-	-	35	µA
Shut-down Current	I_{VINS}		-	-	1	µA
OSCILLATOR						
Oscillator Frequency	f_{OSC}		255	300	345	kHz
Ramp Amplitude, pk-pk	V_{R1}	Vin pin voltage = 16V, by design	-	2	-	V
Ramp Amplitude, pk-pk	V_{R2}	Vin pin voltage = 5V, by design	-	0.625	-	V
Ramp Offset	V_{ROFF}	By design	-	1	-	V
Ramp/V_{IN} Gain	G_{RB1}	Vin pin voltage > 4.2V, by design	-	125	-	mV/V
Ramp/V_{IN} Gain	G_{RB2}	Vin pin voltage ≤ 4.1V, by design	-	250	-	mV/V
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}		-	0.9	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-up	I_{SOFT}		-	4.5	-	µA
Soft-Start Complete Threshold	V_{ST}	By design	-	1.5	-	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM CONVERTERS						
Load Regulation		0.0mA < I_{VOUT1} < 5.0A; 5.0V < V_{IN} < 15.0V	-2.0	-	+2.0	%
VSEN pin bias current	I_{VSEN}	By design	-	80	-	nA
Minimum Duty Cycle	D_{MIN}		-	4	-	%
Maximum Duty Cycle	D_{MAX}		-	87	-	%
Undervoltage Shut-Down Level	V_{UVL}	Fraction of the set point; ~2ms noise filter	70	75	80	%
Overvoltage Protection	V_{OVP1}	Fraction of the set point; ~2ms noise filter	110	115	-	%
GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}	V_{CC} = 5V	-	4	8	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}	V_{CC} = 5V	-	2.3	4	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}	V_{CC} = 5V	-	4	8	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}	V_{CC} = 5V	-	1.1	3	Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power Good Lower Threshold	V_{PG-}	Fraction of the set point; ~3ms noise filter	84	89	92	%
Power Good Higher Threshold	V_{PG+}	Fraction of the set point; ~3ms noise filter.	110	115	120	%
PGOODx Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V	-	-	1	µA
PGOODx Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	0.5	1	V
ISEN sourcing current		By design	-	-	260	µA
OCSET sourcing current range			2	-	20	µA
EN - Low (Off)			-	-	0.8	V
EN - High (On)			2.0	-	-	V
DDR - Low (Off)			-	-	0.8	V
DDR - High (On)			3	-	-	V
DDR REF Output Voltage	V_{DDREF}	DDR = 1, I_{REF} = 0...10mA	0.99* V_{OC2}	V_{OC2}	1.01* V_{OC2}	V
DDR REF Output Current	I_{DDREF}	DDR = 1. Guaranteed by design.	-	10	12	mA

Functional Pin Description

GND (Pin 1, 9, 20)

Signal ground for the IC. All three ground pins must be connected to ground for proper IC operation. Connect to the ground plane through a path as low in inductance as possible.

LGATE1, LGATE2 (Pin 2, 27)

Connect these pins to the gates of the corresponding lower MOSFETs. These pins provide the PWM-controlled gate drive for the lower MOSFETs.

PGND1, PGND2 (Pin 3, 26)

These pins provide the return connection for lower gate drivers, and are connected to sources of the lower MOSFETs of their respective converters. These pins must be connected to the ground plane through a path as low in inductance as possible.

PHASE1, PHASE2 (Pin 4, 25)

The PHASE1 and PHASE2 points are the junction points of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect these pins to the respective converter's upper MOSFET source.

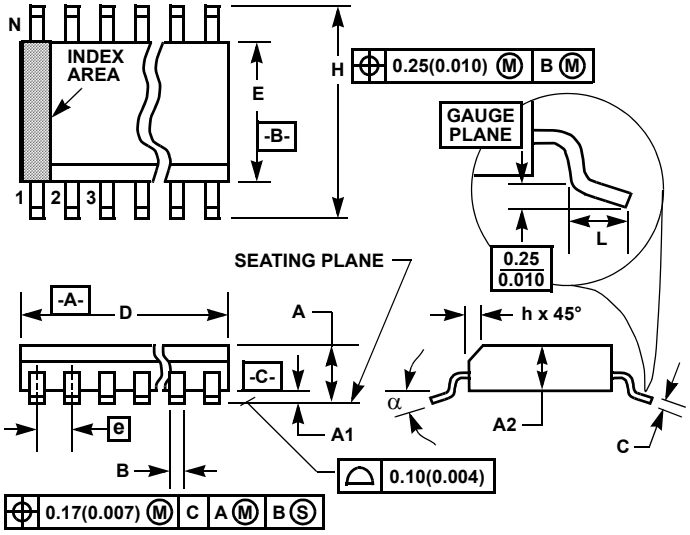
UGATE1, UGATE2 (Pin 5, 24)

Connect these pins to the gates of the corresponding upper MOSFETs. These pins provide the PWM-controlled gate drive for the upper MOSFETs.

BOOT1, BOOT2 (Pin 6, 23)

These pins power the upper MOSFET drivers of the PWM converter. Connect these pins to the junction of the bootstrap capacitor with the cathode of the bootstrap diode. The anode of the bootstrap diode is connected to the VCC voltage.

Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150” WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-