

Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

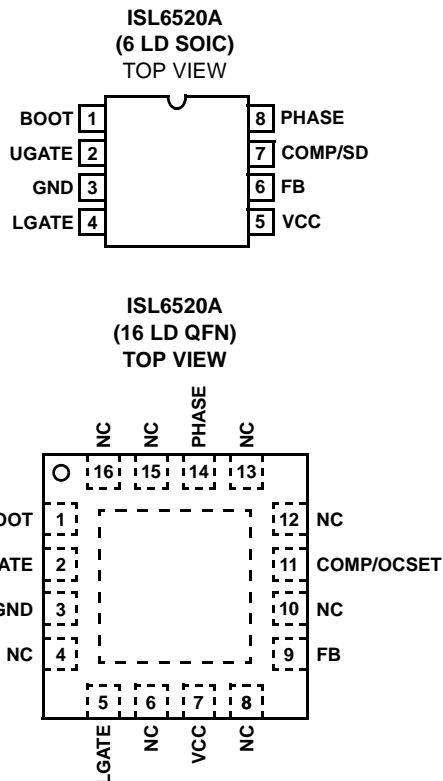
The ISL6520A makes simple work out of implementing a complete control and protection scheme for a DC/DC stepdown converter. Designed to drive N-Channel MOSFETs in a synchronous buck topology, the ISL6520A integrates the control, output adjustment, monitoring and protection functions into a single 8-Lead package.

The ISL6520A provides simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of $\pm 1.5\%$ over-temperature and line voltage variations. A fixed frequency oscillator reduces design complexity, while balancing typical application cost and efficiency.

The error amplifier features a 15MHz gain-bandwidth product and 8V/ms slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty cycles range from 0% to 100%.

Protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

Pinouts



Features

- Operates from +5V Input
- 0.8V to V_{IN} Output Range
 - 0.8V Internal Reference
 - $\pm 1.5\%$ Over Line Voltage and Temperature
- Drives N-Channel MOSFETs
- Simple Single-Loop Control Design
 - Voltage-Mode PWM Control
- Fast Transient Response
 - High-Bandwidth Error Amplifier
 - Full 0% to 100% Duty Cycle
- Lossless, Programmable Overcurrent Protection
 - Uses Upper MOSFET's $r_{DS(ON)}$
- Small Converter Size
 - 300kHz Fixed Frequency Oscillator
 - Internal Soft-Start
 - 8 Ld SOIC or 16 Ld 4mmx4mm QFN
- QFN Package:
 - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
 - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Power Supplies for Microprocessors
 - PCs
 - Embedded Controllers
- Subsystem Power Supplies
 - PCI/AGP/GTL+ Buses
 - ACPI Power Control
 - SSTL-2 and DDR SDRAM Bus Termination Supply
- Cable Modems, Set Top Boxes, and DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 5V-Input DC/DC Regulators
- Low-Voltage Distributed Power Supplies

ISL6520A

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6520ACB*	6520 ACB	0 to +70	8 Ld SOIC	M8.15
ISL6520ACBZ* (Note)	6520 ACBZ	0 to +70	8 Ld SOIC (Pb-free)	M8.15
ISL6520ACBZA* (Note)	6520 ACBZ	0 to +70	8 Ld SOIC (Pb-free)	M8.15
ISL6520AIB*	6520 AIB	-40 to +85	8 Ld SOIC	M8.15
ISL6520AIBZ* (Note)	6520 AIBZ	-40 to +85	8 Ld SOIC (Pb-free)	M8.15
ISL6520ACR*	65 20ACR	0 to +70	16 Ld 4x4mm QFN	L16.4x4
ISL6520ACRZ* (Note)	65 20ACRZ	0 to +70	16 Ld 4x4mm QFN (Pb-free)	L16.4x4
ISL6520AIR*	65 20AIR	-40 to +85	16 Ld 4x4mm QFN	L16.4x4
ISL6520AIRZ * (Note)	65 20AIRZ	-40 to +85	16 Ld 4x4mm QFN (Pb-free)	L16.4x4
ISL6520EVAL1	Evaluation Board			

*Add "-T" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL6520A

Absolute Maximum Ratings

Supply Voltage, V_{CC}	+6.0V
Absolute Boot Voltage, V_{BOOT}	+15.0V
Upper Driver Supply Voltage, $V_{BOOT} - V_{PHASE}$	7.0V (DC) 8.0V (<10ns Pulse Width, 10 μ J)
Input, Output or I/O Voltage	GND -0.3V to $V_{CC} +0.3V$
ESD Classification	Class 2

Operating Conditions

Supply Voltage, V_{CC}	+5V \pm 10%
Ambient Temperature Range - ISL6520AC	0°C to +70°C
Ambient Temperature Range - ISL6520AI	-40°C to +85°C
Junction Temperature Range	-40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	95	N/A
QFN Package (Notes 2, 3)	45	7
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Maximum Lead Temperature (Soldering 10s)	+300°C	
(SOIC - Lead Tips Only)		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

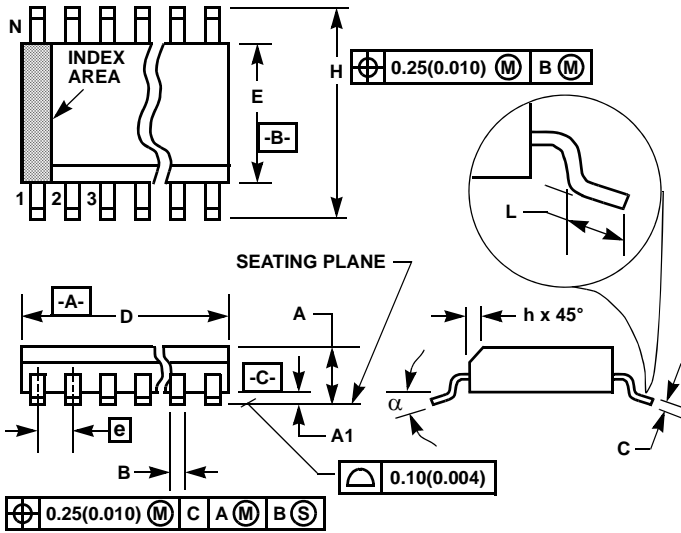
NOTES:

- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{VCC}		2.6	3.2	3.8	mA
POWER-ON RESET						
Rising VCC POR Threshold	POR		4.19	4.30	4.50	V
VCC POR Threshold Hysteresis			-	0.25	-	V
OSCILLATOR						
Frequency	f_{OSC}	ISL6520AC, $V_{CC} = 5V$	250	300	340	kHz
		ISL6520AI, $V_{CC} = 5V$	230	300	340	kHz
Ramp Amplitude	DV_{OSC}		-	1.5	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance		ISL6520AC	-1.5	-	+1.5	%
		ISL6520AI	-2.5	-	+2.5	%
Nominal Reference Voltage	V_{REF}		-	0.800	-	V
ERROR AMPLIFIER						
DC Gain		Guaranteed By Design	-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR		-	8	-	V/ μ s
GATE DRIVERS						
Upper Gate Source Current	$I_{UGATE-SRC}$	$V_{BOOT} - V_{PHASE} = 5V, V_{UGATE} = 4V$	-	-1	-	A
Upper Gate Sink Current	$I_{UGATE-SNK}$		-	1	-	A
Lower Gate Source Current	$I_{LGATE-SRC}$	$V_{VCC} = 5V, V_{LGATE} = 4V$	-	-1	-	A
Lower Gate Sink Current	$I_{LGATE-SNK}$		-	2	-	A
PROTECTION / DISABLE						
OCSET Current Source	I_{OCSET}	ISL6520AC	17	20	22	μ A
		ISL6520AI	14	20	24	μ A
Disable Threshold	$V_{DISABLE}$		-	0.8	-	V

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.