Single Output LNB Supply and Control Voltage Regulator with I^{2}C Interface for Advanced Satellite Set-top Box Designs
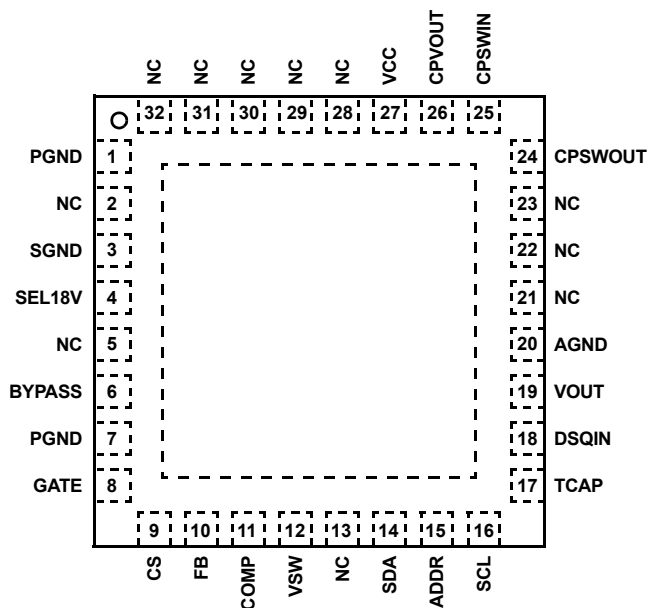
The ISL6421A is a highly integrated solution for providing power and control signals from advanced satellite set-top box (STB) modules to the low noise block (LNB). The internal architecture of this device contains a current-mode boost PWM and a low-noise linear regulator, along with the circuitry required for I^{2}C device interfacing and for providing DiSEqC™ standard control signals to the LNB.

A regulated output voltage is available at the output terminal (VOUT) to support the operation of the antenna port in advanced satellite STB applications. The regulated output may be set to either 13V or 18V by use of the voltage select command bit (VSEL) through the I^{2}C bus. Additionally, to compensate for the voltage drop in the coaxial cable, the voltage may be increased by 1V with the line length compensation bit (LLC) feature. The device can be put into a standby mode by means of the enable bit (EN), this disables the PWM and Linear regulator combination and helps conserve power.

The input to the linear regulator is derived from the current mode boost converter, such that the required voltage is the sum of the output voltage and the linear regulator drop (1.0V typical). This ensures that the power dissipation is minimized and maintains a constant voltage drop across the linear pass element, while permitting an adequate voltage range for tone injection.

The device is capable of providing 450mA (typical). The overcurrent limit is either digitally or resistor programmable.

Features

- Switch-Mode Power Converter for Lowest Dissipation
  - Boost PWM with >92% Efficiency
  - Selectable 13V or 18V Outputs
  - Digital Cable Length Compensation (1V)
  - Vsw tracks Vout ensures low dissipation

- I^{2}C Compatible Interface for Remote Device Control
  - Registered Slave Address 0001 00XX
  - Fully Functional 3.3V, 5V Operation up to 400kHz

- Built-In Tone Oscillator Factory Trimmed to 22kHz
  - Facilitates DiSEqC™ (EUTELSAT) Encoding
  - External Modulation input DSQIN

- Internal Over Temperature Protection and Diagnostics

- Internal Overload and Over Temperature Flags (Visible on I^{2}C)

- Output Back-Bias Protection to 24V

- LNB Short-Circuit Protection and Diagnostics

- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint

- External Pins to Select 13V/18V Options

- Pb-Free Available (RoHS Compliant)

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

References

- Tech Brief 389 (TB389) - "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"; Available on the Intersil website

Pinout

ISL6421A (QFN) TOP VIEW

Ordering Information

PART NUMBER*	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6421AER	ISL6421AER	-20 to 85	32 Ld 5x5 QFN	L32.5x5
ISL6421AERZ (Note)	ISL6421AERZ	-20 to 85	32 Ld 5x5 QFN (Pb-free)	L32.5x5

*Add -T for tape and reel package.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL6421A

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . 8.0V to 18.0V
Logic Input Voltage Range (SDA, SCL, ENT) . . . . -0.5V to 7V
Output Current . . . . Externally/Internally Limited

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package.	35	6

Maximum Junction Temperature . . . . 150°C
Maximum Storage Temperature Range. . . . .-40°C to 150°C

For recommended soldering conditions, see Tech Brief TB389.

NOTE: The device junction temperature should be kept below 150°C. Thermal shut-down circuitry turns off the device if junction temperature exceeds +150°C typically.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

VCC = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. EN = H, LLC = L, ENT = L, DCL = L, DSQIN = L, Iout = 12mA, unless otherwise noted. See software description section for I^{2}C access to the system.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			8	12	14	V
Standby Supply Current		EN = L	-	1.5	3.0	mA
Supply Current	I_{IN}	EN = LLC = VSEL = ENT = H, No Load	-	4.0	8.0	mA
UNDERVOLTAGE LOCKOUT						
Start Threshold			7.5	-	7.95	V
Stop Threshold			7.0	-	7.55	V
Start to Stop Hysteresis			350	400	500	mV
SOFT-START						
COMP Rise Time (Note 3)		(Note 5)	-	1024	-	Cycles
OUTPUT VOLTAGE						
Output Voltage (Note 4)	V_{OUT}	VSEL = L, LLC = L	12.74	13.0	13.26	V
	V_{OUT}	VSEL = L, LLC = H	13.72	14.0	14.28	V
	V_{OUT}	VSEL = H, LLC = L	17.64	18.0	18.36	V
	V_{OOU}	VSEL = H, LLC = H	18.62	19.0	19.38	V
Line Regulation	DV_{OUT}	V_{IN} = 8V to 14V; V_{OUT} = 13V	-	4.0	40.0	mV
		V_{IN} = 8V to 14V; V_{OUT} = 18V	-	4.0	60.0	mV
Load Regulation	DV_{OUT}	I_O = 12mA to 450mA	-	50	80	mV
Dynamic Output Current Limiting	I_{MAX}	DCL = L	500	-	625	mA
Dynamic Overload Protection Off Time	T_{OFF}	DCL = L, Output Shorted (Note 5)	-	900	-	ms
Dynamic Overload Protection On Time	T_{ON}		-	20	-	ms
Output Backward Current	I_{OBK}	EN = 0; V_{OBK} = 24V	-	2.0	3.0	mA
22kHz TONE						
Tone Frequency	f_{tone}	ENT = H	20.0	22.0	24.0	kHz
Tone Amplitude	V_{tone}	ENT = H	500	680	900	mV
Tone Duty Cycle	dc_{tone}	ENT = H	40	50	60	%
Tone Rise or Fall Time	T_r, T_f	ENT = H	5	8	14	µs

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Electrical Specifications VCC = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. EN = H, LLC = L, ENT = L, DCL = L, DSQIN = L, Iout = 12mA, unless otherwise noted. See software description section for I^2C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR						
Drop-out Voltage		Iout = 450mA (Note 5)	-	1.2	-	V
DSQIN PIN						
DSQIN pin logic Low			-	-	1.5V	V
DSQIN pin Logic HIGH			3.5	-	-	V
DSQIN pin Input Current			-	1	-	μA
CURRENT SENSE						
Input Bias Current	I_{BIAS}		-	700	-	nA
Overcurrent Threshold		Static current mode, DCL = H	325	400	500	mV
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{OL}	(Note 5)	70	88	-	dB
Gain Bandwidth Product	GBP	(Note 5)	10	-	-	MHz
PWM						
Maximum Duty Cycle			90	93	-	%
Minimum Pulse Width		(Note 5)	-	20	-	ns
OSCILLATOR						
Oscillator Frequency	f_O	Fixed at (10)(f_{tone})	200	220	240	kHz
THERMAL PROTECTION						
Thermal Shutdown						
Temperature Shutdown Threshold		(Note 5)	-	150	-	°C
Temperature Shutdown Hysteresis		(Note 5)	-	20	-	°C

NOTES:

3. Internal digital soft-start.

4. Voltage programming signals VSEL and LLC are implemented via the I^2C bus.
   IO1 = IO2 = 500mA.

5. Guaranteed by design.

Functional Pin Description

SYMBOL	FUNCTION
SDA	Bidirectional data from/to I^2C bus.
SCL	Clock from I^2C bus.
VSW	Input of the linear post-regulator.
PGND	Dedicated ground for the output gate driver of the PWM.
CS	Current sense input; connect Rsc at this pin for desired overcurrent value for the PWM.
SGND	Small signal ground for the IC.
AGND	Analog ground for the IC.
TCAP	Capacitor for setting rise and fall time of the output of the LNB. Use a capacitor value of 1μF or higher.
BYPASS	Bypass capacitor for internal 5V.
DSQIN	When HIGH this pin enables the internal 22kHz modulation for the LNB, Use this pin for tone enable function for the LNB.

Received Data (I²C Bus Read Mode)

The ISL6421A can provide to the master a copy of the System Register information via the I²C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following Master generated clock bits, the ISL6421A issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

• Acknowledge the reception, starting in this way the transmission of another byte from the ISL6421A.

• Not acknowledge, stopping the read mode communication.

While the whole register is read back by the microprocessor, only the two read-only bits, OLF and OTF, convey diagnostic information about the ISL6421A.

TABLE 6. READING SYSTEM REGISTERS

DCL	ISEL	ENT	LLC	VSEL	EN	OTF	OLF	FUNCTION
These bits are read as they were after the last write operation.						0		$T_j \leq 130°C$, Normal operation
						1		$T_j > 150°C$, Power blocks disabled
							0	Iout < Imax, Normal operation
							1	Iout > Imax, Overload protection triggered

Power-On I²C Interface Reset

The I²C interface built into the ISL6421A is automatically reset at power-on. The I²C interface block will receive a Power OK logic signal from the UVLO circuit. This signal will go HIGH when chip power is OK. As long as this signal is LOW, the interface will not respond to any I²C commands and the system register SR is initialized to all zeros, thus keeping the power blocks disabled.

Once Vcc rises above the UVLO level, the POWER OK signal given to the I²C interface block will be HIGH, the I²C interface becomes operative and the SR can be configured by the main microprocessor. About 400mV of hysteresis is provided in the UVLO threshold to avoid false triggering of the Power-On reset circuit.

(I²C comes up with EN = 0, EN goes HIGH at the same time as (or later than) all other I²C data for the PWM becomes valid).

ADDRESS Pin

Connecting this pin to GND forces the chip I²C interface address to 0001000; applying a voltage >2.7V forces the address to 0001001, as shown below.

TABLE 7. ADDRESS PIN CHARACTERISTICS

Vaddr	MIN	TYP	MAX
Vaddr-1 "0001000"	0V	-	2.0V
Vaddr-2 "0001001"	2.7V	-	5.0V

I²C Electrical Specifications

TABLE 8. I²C SPECIFICATIONS

PARAMETER	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Input Logic High, VIH	SDA, SCL		$0.7 \times V_{DD}$	
Input Logic Low, VIL	SDA, SCL		$0.3 \times V_{DD}$	
Input Logic Current, IIL	SDA, SCL; 0.4V < Vin < 4.5V			10μA
SCL Clock Frequency		0	100kHz	400kHz

NOTE: V_{DD} = 5.0V/3.3V.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)

TOP VIEW

SIDE VIEW

BOTTOM VIEW

SECTION "C-C"

FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE

L32.5x5
**32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C**
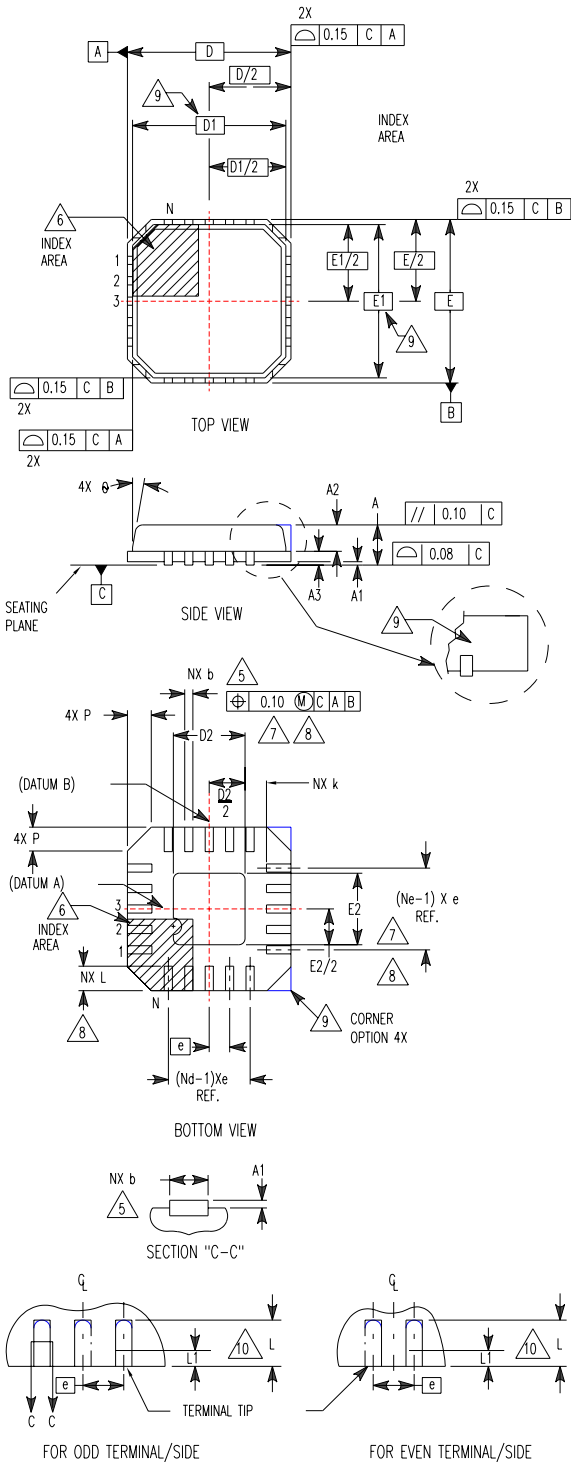
| SYMBOL | MILLIMETERS | | | NOTES |
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.18	0.23	0.30	5,8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	2.95	3.10	3.25	7,8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	2.95	3.10	3.25	7,8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N	32			2
Nd	8			3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.

2. N is the number of terminals.

3. Nd and Ne refer to the number of terminals on each D and E.

4. All dimensions are in millimeters. Angles are in degrees.

5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.

8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.

9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.

10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.
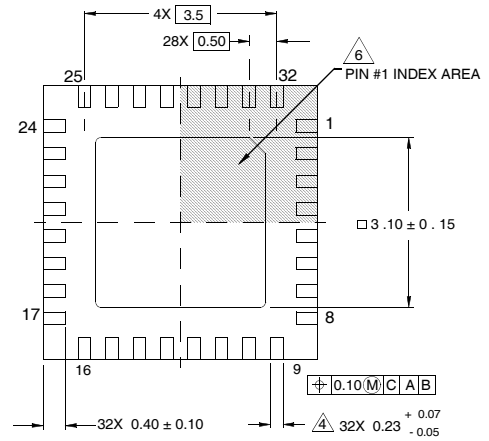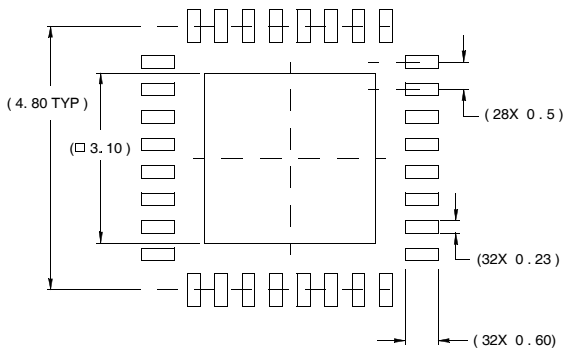
Package Outline Drawing

L32.5x5
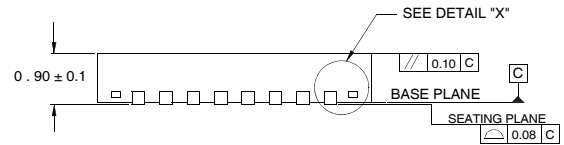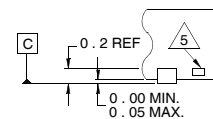**32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
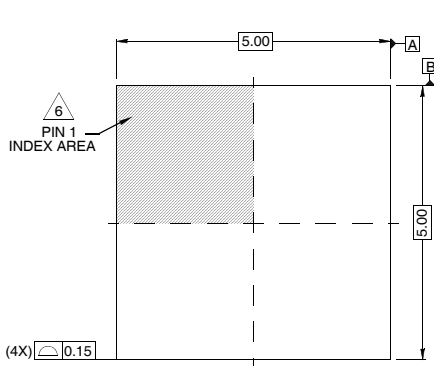
TOP VIEW

BOTTOM VIEW

TYPICAL RECOMMENDED LAND PATTERN

SIDE VIEW

DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.