Multiple Voltage Supervisory ICs

The ISL6131 and ISL6132 are a family of high accuracy multi voltage supervisory ICs designed to monitor voltages greater than 0.7V in applications ranging from microprocessors to industrial power systems. The **ISL6131** is an undervoltage four supply supervisor whereas the **ISL6132** is a two voltage supervisor monitoring both for undervoltage (UV) and overvoltage (OV) conditions.

Both ICs feature four external resistor programmable voltage monitoring (VMON) inputs each with a related STATUS output that individually reports the related monitor input condition. In addition there is a PGOOD (power good) signal that asserts high when the STATUS outputs are in their correct state. There is a stability delay of approximately 160ms to ensure that the monitored supply is stable before STATUS and PGOOD are released to go high. The PGOOD and STATUS outputs are open-drain to allow ORing of the signals and interfacing to a wide range of logic levels.

STATUS and PGOOD outputs are guaranteed to be valid with IC bias lower than 1V eliminating concern about STATUS and PGOOD outputs during IC bias up and down. VMON inputs are designed to ignore momentary transients on the monitored supplies.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6131IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6132IR	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6131IRZA (Note)	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL6132IRZA (Note)	-40 to +85	24 Ld 4x4 QFN (Pb-free)	L24.4x4
ISL613XSUPEREVAL2	Evaluation Platform		

Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Operates from 1.5V to 5.5V Supply Voltage
- Four Adjustable Voltage Monitoring Thresholds
- 150ms STATUS/PGOOD Stability Time Delay
- Four Individual Open Drain STATUS Outputs
- Guaranteed STATUS/PGOOD Valid to V_{DD} <1V
- V_{DD} and VMON Glitch Immunity
- V_{DD} Lock Out
- 4mm X 4mm QFN Package
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Multivoltage DSPs and Processors
- µP Voltage Monitoring
- Embedded Control Systems
- Graphics Cards
- Intelligent Instruments
- Medical Equipment
- Network Routers
- Portable Battery-Powered Equipment
- Set-Top Boxes
- Telecommunications Systems

Absolute Maximum Ratings

V_{DD} . . . . . +6.0V
VMON, ENABLE, STATUS, PGOOD. . . . . -0.3V to V_{DD}+0.3V
ESD Classification . . . . . 2kV (HBM)

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +1.5V to +5.5V
Temperature Range (T_A) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package	48	9

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(QFN - Leads Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal V_{DD} = 1.5V to +5V, T_A = T_J = -40°C - 85°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMON/ENABLE INPUTS						
VMON Threshold	$V_{VMONvth}$	T_J = 25°C	619	633	647	mV
VMON Threshold Temp. Coeff.	$TC_{VMONvth}$	T_J from -40°C to +85°C	-	40	-	nV/°C
VMON Hysteresis	$V_{VMONhys}$		-	10	-	mV
VMON Glitch Filter	Tfil		-	30	-	µs
VMON Minimum Input Impedance	Zin_min	Tj = 40°C, VMON within 63mV of $V_{VMONvth}$		8		MΩ
ENABLE L2H, Delay to STATUS & PGOOD		VMON valid, EN high to STATUS & PG high	-	160	-	ms
EN H2L, Delay to PGOOD		EN low to PGOOD low	-	-	0.1	µs
EN H2L, Delay to STATUS		EN low to STATUS low	-	13	-	µs
ENABLE Pull-up Voltage		EN open	-	V_{DD}	-	V
ENABLE Threshold Voltage	VENVTH		-	V_{DD}/2	-	V
STATUS/PGOOD OUTPUTS						
STATUS Pull-Down Current	$I_{\overline{RST}pd}$	$\overline{RST}$ = 0.1V	-	88	-	mA
STATUS/PGOOD Delay after VMON Valid	T_{delST}	VMON > V_{UVvth} to STATUS = 0.2V	-	160	-	ms
STATUS/PGOOD Output Low	Vol	Measured at V_{DD} = 1.0V	-	0.04	0.1	V
BIAS						
IC Supply Current	$I_{VDD\_5.5V}$	V_{DD} = 5V	-	170	-	µA
IC Supply Current	$I_{VDD\_3.3V}$	V_{DD} = 3.3V	-	145	-	µA
IC Supply Current	$I_{VDD\_1.5V}$	V_{DD} = 1.5V	-	100	-	µA
V_{DD} Power On	V_{DD}_POR	V_{DD} high to low	-	0.89	1	V
V_{DD} Power On Lock Out	V_{DD}_LO	V_{DD} low to high	-	0.91	-	V

Description and Operation

The **ISL6131** is a four voltage high accuracy supervisory IC designed to monitor multiple voltages greater than 0.7V relative to PIN 10 of the IC.

Upon V_{DD} bias power up, the STATUS and PGOOD outputs are held correctly low once V_{DD} is as low as 1V. Once biased to 1.5V the IC continuously monitors from one to four voltages independently through external resistor dividers comparing each voltage monitoring (VMON) pin voltage to an internal 0.633V ($V_{VMONvth}$) reference.

With the EN input driven high or open as each VMON input rises above $V_{VMONvth}$ a timer is set to ensure ~160ms of continuous compliance then the related STATUS output is released to be pulled high. The STATUS outputs are open-drain to allow ORing of these signals and interfacing to a logic high level up to V_{DD}. The STATUS are designed to reject short transients (~30µs) on the VMON inputs. Once all STATUS outputs are high a power good (PGOOD) output signal is generated high to indicate all the monitored voltages are greater than minimum compliance level.

Once any VMON input falls below $V_{VMONvth}$ for longer than the glitch filter time both the PGOOD and the related STATUS output are pulled low. The other STATUS outputs will remain high as long as their corresponding VMON voltage remains valid and the PGOOD validation process is reset.

Figure 1 illustrates **ISL6131** typical application schematic and Figure 3 is an operational timing diagram. See Figures 10 to 17 for **ISL6131** function and performance. Figures 10 and 11 show the V_{DD} rising along with STATUS and PGOOD response. Figures 12 and 13 illustrate VMON falling below $V_{VMONvth}$ and Figure 14 illustrates VMON rising above $V_{VMONvth}$ with STATUS and PGOOD response. Figure 15 shows the V_{DD} failing with STATUS and PGOOD response. Figures 16 and 17 illustrate ENABLE to STATUS and PGOOD timing.

If less than four voltages are being monitored, connect the unused VMON pins to V_{DD} for proper operation. All unused STATUS outputs can be left open.

The **ISL6132** is a dual voltage monitor for under and overvoltage compliance. Figure 2 illustrates the typical **ISL6132** implementation schematic and Figure 4 is the operational timing diagram.

There are 2 pairs of monitors each with an undervoltage (UVMON) input and overvoltage (OVMON) input along with with associated STATUS and PGOOD outputs.

Upon V_{DD} bias power up, the STATUS and PGOOD outputs are held correctly low once V_{DD} is as low as 1V. Once biased to 1.5V the IC continuously monitors the voltage through external resistor dividers comparing each VMON pin voltage to an internal 0.633V reference. At proper bias the OVSTATUS are pulled high and the UVSTATUS and PGOOD are pulled low. Once the UVMON input > the VMON Vth continuously for ~160ms, its associated STATUS output will release high indicating that the minimum voltage condition has been met. As both UVMON and OVMON inputs are satisfied the PGOOD output is released to go high indicating that the monitored voltage is within the specified window. Figure 18 illustrates this performance for a 4V to 5V window.

When VMON does not satisfy its voltage high or low criteria for more than the glitch filter time, the associated STATUS and PGOOD are pulled low. Figures 19 and 20 illustrate this performance for a 4V to 5V compliant window.

Figures 21-23 illustrate the VMON glitch filter timing to STATUS and PGOOD notification and transient immunity.

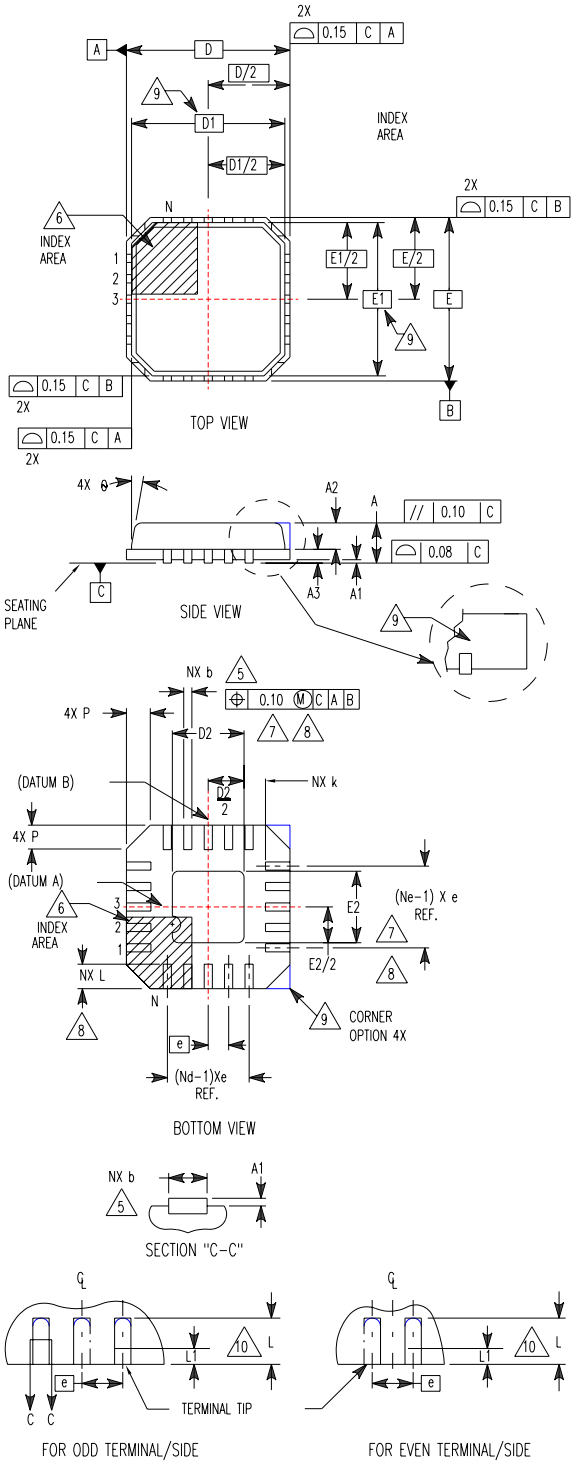
The ENABLE input when pulled low allows for monitoring and reporting function to be disabled. Figure 24 shows ENABLE high to PGOOD timing for compliant voltage.

When choosing resistors for the divider remember to keep the current through the string bounded by power loss tolerance at the top end and noise immunity at the bottom end. For most applications total divider resistance in the 10kΩ -100kΩ range is advisable with 1% tolerance resistors being used to reduce monitoring error.

Referencing Figures 1 and 2, choosing the two resistor values is straightforward for the ISL6131 as the ratio of resistance should equal the ratio of the desired trip voltage to the internal reference, 0.633V).
For the ISL6131, two dividers of two resistors each can be employed to monitor the OV and UV levels for each voltage. Otherwise, use a single three resistor string for each voltage. In the three resistor divider string the ratio of the desired over voltage trip point to the internal reference is equal to the ratio of the two upper resistors to the lowest (gnd connected) resistor. The desired under voltage trip point ratio to the internal reference voltage is equal to the ratio of the uppermost (voltage connected) resistor to the lower two resistors. An example follows;

1. Establish lower and upper trip level: 3.3V ±20% or 2.64V (UV) and 3.96V (OV)
2. Establish total resistor string value: 10kΩ, Ir = divider current
3. (Rm+Rl)*Ir = 0.623V @ UV and Rl * Ir = 0.633V @ OV
4. Rm+Rl = 0.623V / Ir @ UV => Rm+Rl = 0.623V / (2.64V /10kΩ) = 2.359kΩ
5. Rl = 0.633V / Ir @ OV => Rl = 0.633V /(3.96V/10kΩ) = 1.598kΩ
6. Rm = 2.359kΩ - 1.598kΩ = 0.761kΩ
7. Ru = 10kΩ - 2.397kΩ = 7.641kΩ
8. Choose standard value resistors that most closely approximate these ideal values. Choosing a different total divider resistance value may yield a more ideal ratio with available resistors values.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L24.4x4

24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		24		2
Nd		6		3
Ne		6		3
P	-	-	0.60	9
θ	-	-	12	9

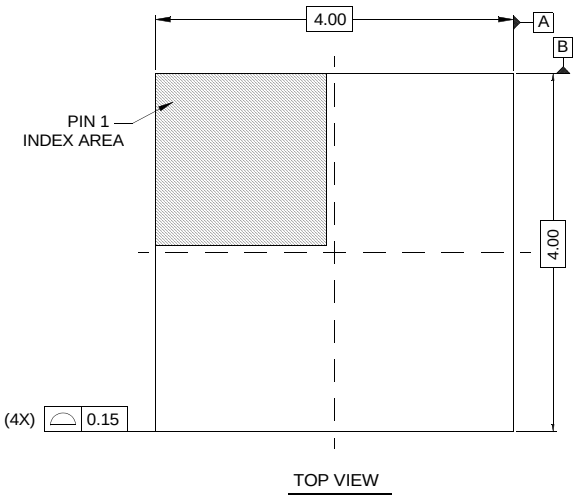
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

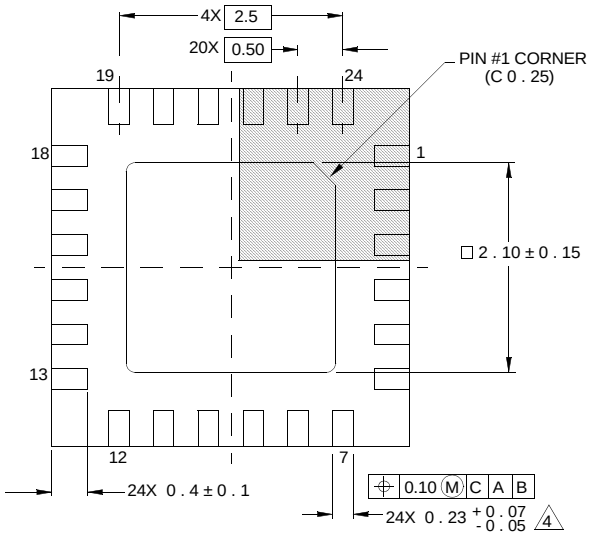
Package Outline Drawing

L24.4x4

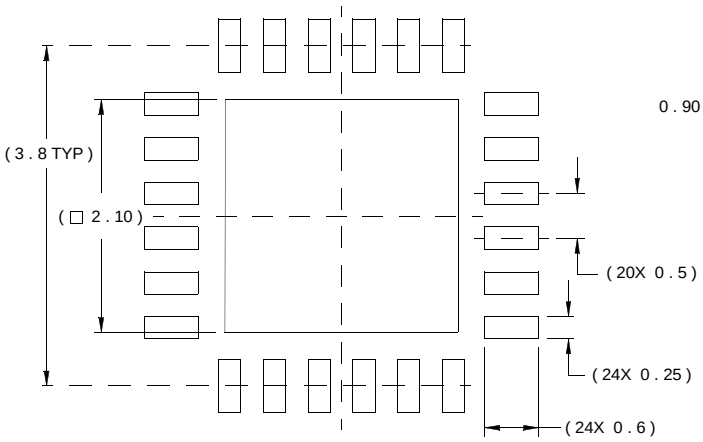
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



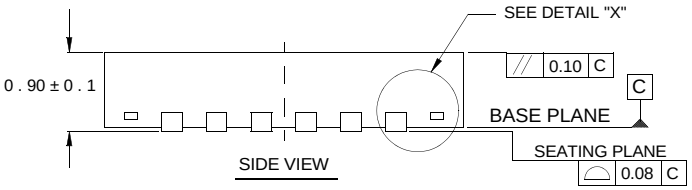
TOP VIEW



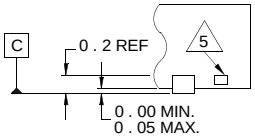
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.