

## Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Datasheet Describes Mode 0 Operation
- Low-voltage and Standard-voltage Operation
  - 2.7 ( $V_{CC} = 2.7V$  to 5.5V)
  - 1.8 ( $V_{CC} = 1.8V$  to 5.5V)
- 20 MHz Clock Rate (5V)
- 32-byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect (WP) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (5 ms max)
- High Reliability
  - Endurance: One Million Write Cycles
  - Data Retention: 100 Years
- Available in Automotive
- 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-lead MAP, 8-lead Ultra Thin Mini-MAP (MLP 2x3) and 8-lead TSSOP Packages
- Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers

## Description

The AT25080A/160A/320A/640A provides 8192/16384/32768/65536 bits of serial electrically-erasable programmable read-only memory (EEPROM) organized as 1024/2048/4096/8192 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25080A/160A/320A/640A is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP, 8-lead Ultra Thin Mini-MAP (MLP 2x3), 8-lead TSSOP and 8-Lead Ultra Leadframe Land Grid Array (ULLGA) packages.

The AT25080A/160A/320A/640A is enabled through the Chip Select pin ( $\overline{CS}$ ) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.



## SPI Serial EEPROMs

**8K (1024 x 8)**

**16K (2048 x 8)**

**32K (4096 x 8)**

**64K (8192 x 8)**

**AT25080A**

**AT25160A**

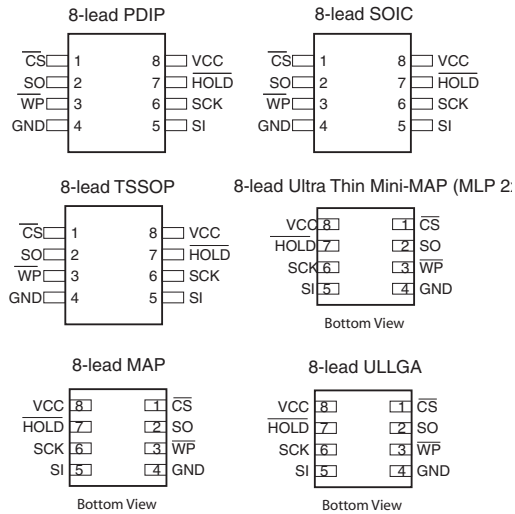
**AT25320A**

**AT25640A**



**Table 0-1. Pin Configuration**

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect
DC	Don't Connect



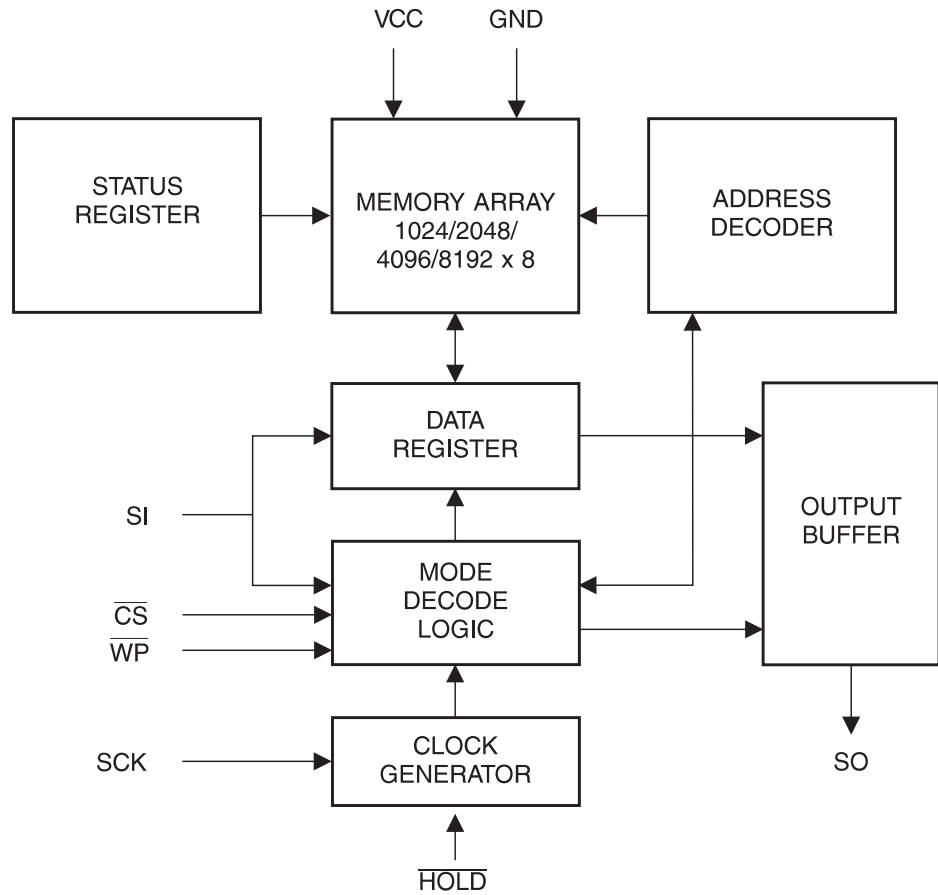
Block write protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the  $\overline{WP}$  pin to protect against inadvertent write attempts to the status register. The  $\overline{HOLD}$  pin may be used to suspend any serial communication without resetting the serial sequence.

## 1. Absolute Maximum Ratings\*

Operating Temperature.....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0V to +7.0V
Maximum Operating Voltage .....	6.25V
DC Output Current.....	5.0 mA

**\*NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 1-1.** Block Diagram



**Table 1-1.** Pin Capacitance<sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +5.0\text{V}$  (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
$C_{OUT}$	Output Capacitance (SO)	8	pF	$V_{OUT} = 0\text{V}$
$C_{IN}$	Input Capacitance ( $\overline{CS}$ , SCK, SI, $\overline{WP}$ , HOLD)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

**Table 1-2. DC Characteristics**

 Applicable over recommended operating range from:  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$  (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{CC1}$	Supply Voltage		1.8		5.5	V
$V_{CC2}$	Supply Voltage		2.7		5.5	V
$V_{CC3}$	Supply Voltage		4.5		5.5	V
$I_{CC1}$	Supply Current	$V_{CC} = 5.0\text{V}$ at 20 MHz, SO = Open, Read		7.5	10.0	mA
$I_{CC2}$	Supply Current	$V_{CC} = 5.0\text{V}$ at 20 MHz, SO = Open, Read, Write		4.0	10.0	mA
$I_{CC3}$	Supply Current	$V_{CC} = 5.0\text{V}$ at 5 MHz, SO = Open, Read, Write		4.0	6.0	mA
$I_{SB1}$	Standby Current	$V_{CC} = 1.8\text{V}$ , $\overline{CS} = V_{CC}$		< 0.1	6.0 <sup>(2)</sup>	$\mu\text{A}$
$I_{SB2}$	Standby Current	$V_{CC} = 2.7\text{V}$ , $\overline{CS} = V_{CC}$		0.3	7.0 <sup>(2)</sup>	$\mu\text{A}$
$I_{SB3}$	Standby Current	$V_{CC} = 5.0\text{V}$ , $\overline{CS} = V_{CC}$		2.0	10.0 <sup>(2)</sup>	$\mu\text{A}$
$I_{IL}$	Input Leakage	$V_{IN} = 0\text{V}$ to $V_{CC}$	-3.0		3.0	$\mu\text{A}$
$I_{OL}$	Output Leakage	$V_{IN} = 0\text{V}$ to $V_{CC}$ , $T_{AC} = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	-3.0		3.0	$\mu\text{A}$
$V_{IL}^{(1)}$	Input Low-voltage		-0.6		$V_{CC} \times 0.3$	V
$V_{IH}^{(1)}$	Input High-voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
$V_{OL1}$	Output Low-voltage	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$			0.4	V
$V_{OH1}$	Output High-voltage		$I_{OL} = 3.0\text{ mA}$			V
$V_{OL2}$	Output Low-voltage	$1.8\text{V} \leq V_{CC} \leq 3.6\text{V}$		$V_{CC} - 0.8$		V
$V_{OH2}$	Output High-voltage		$I_{OH} = -1.6\text{ mA}$			V
					0.2	V
			$V_{CC} - 0.2$			V

- Notes: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.  
 2. Worst case measured at  $85^{\circ}\text{C}$

**Table 1-3.** AC Characteristics

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = \text{As Specified}$ ,  
 $CL = 1$  TTL Gate and  $30\text{ pF}$  (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
$f_{SCK}$	SCK Clock Frequency	4.5–5.5	0	20	MHz
		2.7–5.5	0	10	
		1.8–5.5	0	5	
$t_{RI}$	Input Rise Time	4.5–5.5		2	$\mu\text{s}$
		2.7–5.5		2	
		1.8–5.5		2	
$t_{FI}$	Input Fall Time	4.5–5.5		2	$\mu\text{s}$
		2.7–5.5		2	
		1.8–5.5		2	
$t_{WH}$	SCK High Time	4.5–5.5	20		ns
		2.7–5.5	40		
		1.8–5.5	80		
$t_{WL}$	SCK Low Time	4.5–5.5	20		ns
		2.7–5.5	40		
		1.8–5.5	80		
$t_{CS}$	$\overline{CS}$ High Time	4.5–5.5	25		ns
		2.7–5.5	50		
		1.8–5.5	100		
$t_{CSS}$	$\overline{CS}$ Setup Time	4.5–5.5	25		ns
		2.7–5.5	50		
		1.8–5.5	100		
$t_{CSH}$	$\overline{CS}$ Hold Time	4.5–5.5	25		ns
		2.7–5.5	50		
		1.8–5.5	100		
$t_{SU}$	Data In Setup Time	4.5–5.5	5		ns
		2.7–5.5	10		
		1.8–5.5	20		
$t_{HI}$	Data In Hold Time	4.5–5.5	5		ns
		2.7–5.5	10		
		1.8–5.5	20		
$t_{HD}$	$\overline{HOLD}$ Setup Time	4.5–5.5	5		
		2.7–5.5	10		
		1.8–5.5	20		
$t_{CD}$	$\overline{HOLD}$ Hold Time	4.5–5.5	5		ns
		2.7–5.5	10		
		1.8–5.5	20		
$t_V$	Output Valid	4.5–5.5	0	20	ns
		2.7–5.5	0	40	
		1.8–5.5	0	80	
$t_{HO}$	Output Hold Time	4.5–5.5	0		ns
		2.7–5.5	0		
		1.8–5.5	0		

**Table 1-3.** AC Characteristics (Continued)

Applicable over recommended operating range from  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = \text{As Specified}$ ,  
 $CL = 1$  TTL Gate and  $30$  pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
$t_{LZ}$	$\overline{\text{HOLD}}$ to Output Low Z	4.5–5.5	0	25	ns
		2.7–5.5	0	50	
		1.8–5.5	0	100	
$t_{HZ}$	$\overline{\text{HOLD}}$ to Output High Z	4.5–5.5		40	ns
		2.7–5.5		80	
		1.8–5.5		200	
$t_{DIS}$	Output Disable Time	4.5–5.5		40	ns
		2.7–5.5		80	
		1.8–5.5		200	
$t_{WC}$	Write Cycle Time	4.5–5.5		5	ms
		2.7–5.5		5	
		1.8–5.5		5	
Endurance <sup>(1)</sup>	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

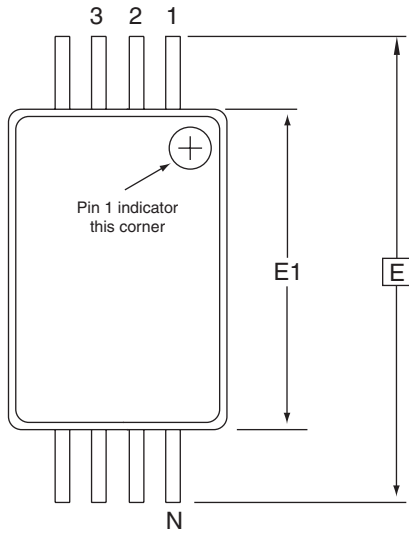
## 8. AT25640A Ordering Information<sup>(1)</sup>

Ordering Code	Package	Operation Range
AT25640A-10PU-2.7 <sup>(2)</sup>	8P3	Lead-free/Halogen-free/ Industrial Temperature (-40 to 85°C)
AT25640A-10PU-1.8 <sup>(2)</sup>	8P3	
AT25640AN-10SU-2.7 <sup>(2)</sup>	8S1	
AT25640AN-10SU-1.8 <sup>(2)</sup>	8S1	
AT25640A-10TU-2.7 <sup>(2)</sup>	8A2	
AT25640A-10TU-1.8 <sup>(2)</sup>	8A2	
AT25640AY1-10YU-1.8 <sup>(2)</sup> (Not recommended for new design)	8Y1	
AT25640AY6-10YH-1.8 <sup>(3)</sup>	8Y6	
AT25640A-W1.8-11 <sup>(3)</sup>	Die Sale	Industrial Temperature (-40 to 85°C)

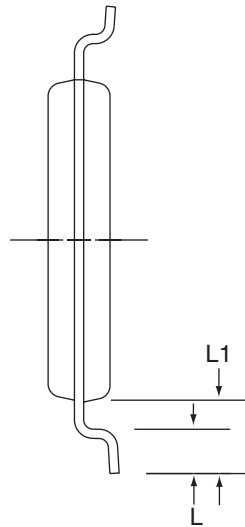
- Notes:
1. For 2.7V devices used in the 4.5 to 5.5V range, please refer to performance values in the AC and DC Characteristics tables.
  2. "U" designates Green package + RoHS compliant.
  3. "H" designates Green package + RoHS compliant, with NiPdAu Lead Finish.
  4. Available in waffle pack and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial EEPROM Marketing.

Package Type	
<b>8P3</b>	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8A2</b>	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
<b>8Y1</b>	8-lead, 4.90 mm x 3.00 mm Body, Dual Footprint, Non-leaded, Miniature Array Package (MAP)
<b>8Y6</b>	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm)
Options	
<b>-2.7</b>	Low Voltage (2.7 to 5.5V)
<b>-1.8</b>	Low Voltage (1.8 to 5.5V)

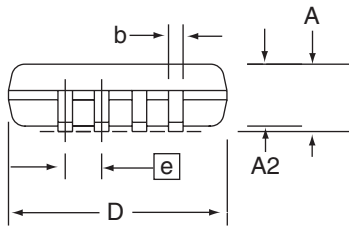
8A2 – TSSOP



Top View



End View



Side View

**COMMON DIMENSIONS**  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	-	-	1.20	
A2	0.80	1.00	1.05	
b	0.19	-	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

**ATMEL** 2325 Orchard Parkway  
San Jose, CA 95131

**TITLE**  
**8A2**, 8-lead, 4.4 mm Body, Plastic  
Thin Shrink Small Outline Package (TSSOP)

**DRAWING NO.**  
8A2

**REV.**  
B