National Semiconductor

LP3961/LP3964
800mA Fast Ultra Low Dropout Linear Regulators

General Description

The LP3961/LP3964 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very fast to step changes in load which makes them suitable for low voltage microprocessor applications. The LP3961/LP3964 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3961/LP3964 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 24mV at 80mA load current and 240mV at 800mA load current.

Ground Pin Current: Typically 4mA at 800mA load current.

Shutdown Mode: Typically 15µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3961).

SENSE: Sense pin improves regulation at remote loads. (For LP3964)

Precision Output Voltage: Multiple output voltage options are available ranging from 1.2V to 5.0V and adjustable (LP3964), with a guaranteed accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

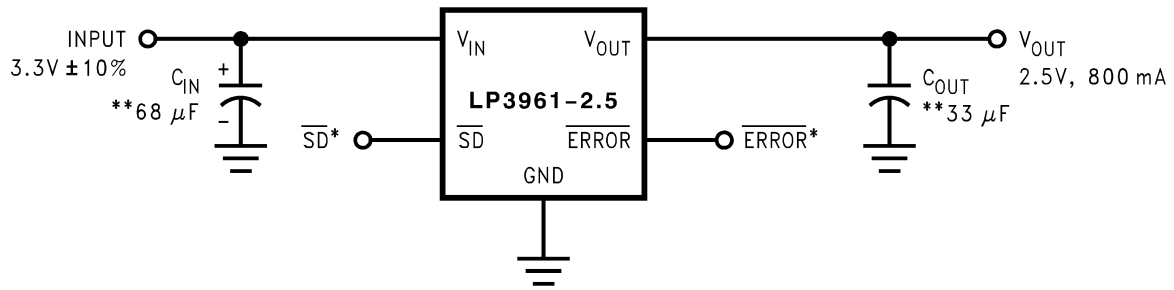
Features

- Ultra low dropout voltage
- Low ground pin current
- Load regulation of 0.02%
- 15µA quiescent current in shutdown mode
- Guaranteed output current of 0.8A DC
- Available in SOT-223,TO-263 and TO-220 packages
- Output voltage accuracy ± 1.5%
- $\overline{\text{Error}}$ flag indicates output status (LP3961)
- Sense option improves better load regulation (LP3964)
- Extremely low output capacitor requirements
- Overtemperature/overcurrent protection
- −40˚C to +125˚C junction temperature range

Applications

- Microprocessor power supplies
- GTL, GTL+, BTL, and SSTL bus terminators
- Power supplies for DSPs
- SCSI terminator
- Post regulators
- High efficiency linear regulators
- Battery chargers
- Other battery powered applications

Typical Application Circuits



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*$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints.

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
5.0	LP3961EMP-5.0	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBSB	1000 units on Tape and Reel
5.0	LP3961EMPX-5.0	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBSB	2000 units on Tape and Reel
3.3	LP3961EMP-3.3	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LAZB	1000 units on Tape and Reel
3.3	LP3961EMPX-3.3	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LAZB	2000 units on Tape and Reel
2.5	LP3961EMP-2.5	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBBB	1000 units on Tape and Reel
2.5	LP3961EMPX-2.5	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBBB	2000 units on Tape and Reel
1.8	LP3961EMP-1.8	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBAB	1000 units on Tape and Reel
1.8	LP3961EMPX-1.8	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBAB	2000 units on Tape and Reel
5.0	LP3964EMP-5.0	800mA, SENSE	SOT223-5	LBUB	1000 units on Tape and Reel
5.0	LP3964EMPX-5.0	800mA, SENSE	SOT223-5	LBUB	2000 units on Tape and Reel
3.3	LP3964EMP-3.3	800mA, SENSE	SOT223-5	LBJB	1000 units on Tape and Reel
3.3	LP3964EMPX-3.3	800mA, SENSE	SOT223-5	LBJB	2000 units on Tape and Reel
2.5	LP3964EMP-2.5	800mA, SENSE	SOT223-5	LBHB	1000 units on Tape and Reel
2.5	LP3964EMPX-2.5	800mA, SENSE	SOT223-5	LBHB	2000 units on Tape and Reel
1.8	LP3964EMP-1.8	800mA, SENSE	SOT223-5	LBFB	1000 units on Tape and Reel
1.8	LP3964EMPX-1.8	800mA, SENSE	SOT223-5	LBFB	2000 units on Tape and Reel
ADJ	LP3964EMP-ADJ	800mA, ADJ	SOT223-5	LBPB	1000 units on Tape and Reel
ADJ	LP3964EMPX-ADJ	800mA, ADJ	SOT223-5	LBPB	2000 units on Tape and Reel
5.0	LP3961ES-5.0	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-5.0	Rail
5.0	LP3961ESX-5.0	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ESX-5.0	Tape and Reel
3.3	LP3961ES-3.3	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-3.3	Rail
3.3	LP3961ESX-3.3	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-3.3	Tape and Reel
2.5	LP3961ES-2.5	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-2.5	Rail
2.5	LP3961ESX-2.5	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-2.5	Tape and Reel
1.8	LP3961ES-1.8	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-1.8	Rail
1.8	LP3961ESX-1.8	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-1.8	Tape and Reel
5.0	LP3964ES-5.0	800mA, SENSE	TO263-5	LP3964ES-5.0	Rail
5.0	LP3964ESX-5.0	800mA, SENSE	TO263-5	LP3964ES-5.0	Tape and Reel
3.3	LP3964ES-3.3	800mA, SENSE	TO263-5	LP3964ES-3.3	Rail
3.3	LP3964ESX-3.3	800mA, SENSE	TO263-5	LP3964ES-3.3	Tape and Reel
2.5	LP3964ES-2.5	800mA, SENSE	TO263-5	LP3964ES-2.5	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 5 sec.)	260˚C
ESD Rating (Note 3)	2 kV
Power Dissipation (Note 2)	Internally Limited
Input Supply Voltage (Survival)	−0.3V to +7.5V
Shutdown Input Voltage (Survival)	−0.3V to V_{IN}+0.3V
Output Voltage (Survival), (Note 6), (Note 7)	−0.3V to +7.5V
I_{OUT} (Survival)	Short Circuit Protected
Maximum Voltage for $\overline{\text{ERROR}}$ Pin	V_{IN}+0.3V
Maximum Voltage for SENSE Pin	V_{OUT}+0.3V

Operating Ratings

Input Supply Voltage (Operating), (Note 12)	2.5V to 7.0V
Shutdown Input Voltage (Operating)	−0.3V to V_{IN}+0.3V
Maximum Operating Current (DC)	0.8A
Operating Junction Temp. Range	−40˚C to +125˚C

Electrical Characteristics LP3961/LP3964

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} = 33µF, $V_{SD} = V_{IN}$-0.3V.

Symbol	Parameter	Conditions	Typ (Note 4)	LP3961/4 (Note 5) Min	LP3961/4 (Note 5) Max	Units
V_O	Output Voltage Tolerance (Note 8)	10 mA ≤ I_L ≤ 800mA V_{OUT} +1 ≤ V_{IN}≤ 7.0V	0	-1.5 **-3.0**	+1.5 **+3.0**	%
V_{ADJ}	Adjust Pin Voltage (ADJ version)	10 mA ≤ I_L ≤ 800mA V_{OUT} +1.5V ≤ V_{IN}≤ 7.0V	1.216	1.198 **1.180**	1.234 **1.253**	V
ΔV_{OL}	Output Voltage Line Regulation (Note 8)	V_{OUT}+1V<V_{IN}<7.0V	0.02 **0.06**			%
$\Delta V_O / \Delta I_{OUT}$	Output Voltage Load Regulation (Note 8)	10 mA < I_L < 800 mA	0.02 **0.08**			%
V_{IN} - V_{OUT}	Dropout Voltage (Note 10)	I_L = 80 mA	24		30 **35**	mV
		I_L = 800 mA	240		300 **350**	
I_{GND}	Ground Pin Current In Normal Operation Mode	I_L = 80 mA	3		9 **10**	mA
		I_L = 800 mA	4		14 **15**	
I_{GND}	Ground Pin Current In Shutdown Mode (Note 11)	V_{SD} ≤ 0.2V	15		25 **75**	µA
$I_{O(PK)}$	Peak Output Current	(Note 2)	1.5	1.2 **1.1**		A
SHORT CIRCUIT PROTECTION						
I_{SC}	Short Circuit Current		2.8			A
OVER TEMPERATURE PROTECTION						
Tsh(t)	Shutdown Threshold		165			˚C
Tsh(h)	Thermal Shutdown Hysteresis		10			˚C
SHUTDOWN INPUT						
V_{SDT}	Shutdown Threshold	Output = High	V_{IN}	**V_{IN}−0.3**		V
		Output = Low	0		**0.2**	

Electrical Characteristics
LP3961/LP3964 (Continued)

Limits in standard typeface are for T_J = 25˚C, and limits in **boldface type** apply over the **full operating temperature range**. Unless otherwise specified: $V_{IN} = V_{O(NOM)}$ + 1V, I_L = 10 mA, C_{OUT} = 33µF, $V_{SD} = V_{IN}$-0.3V.

Symbol	Parameter	Conditions	Typ (Note 4)	LP3961/4 (Note 5)		Units
				Min	Max	
T_{dOFF}	Turn-off delay	I_L = 800 mA	20			µs
T_{dON}	Turn-on delay	I_L = 800 mA	25			µs
I_{SD}	$\overline{SD}$ Input Current	$V_{SD} = V_{IN}$	1			nA
ERROR FLAG COMPARATOR						
V_T	Threshold	(Note 9)	10	**5**	**16**	%
V_{TH}	Threshold Hysteresis	(Note 9)	5	**2**	**8**	%
$V_{EF(Sat)}$	$\overline{Error}$ Flag Saturation	I_{sink} = 100µA	0.02		**0.1**	V
Td	Flag Reset Delay		1			µs
I_{lk}	$\overline{Error}$ Flag Pin Leakage Current		1			nA
I_{max}	$\overline{Error}$ Flag Pin Sink Current	V_{Error} = **0.5V** (over temp.)	1			mA
AC PARAMETERS						
PSRR	Ripple Rejection	$V_{IN} = V_{OUT}$ + 1.5V C_{OUT} = 100uF V_{OUT} = 3.3V	60			dB
		$V_{IN} = V_{OUT}$ + 0.3V C_{OUT} = 100uF V_{OUT} = 3.3V	40			
$\rho_{n(l/f}$	Output Noise Density	f = 120Hz	0.8			µV
e_n	Output Noise Voltage (rms)	BW = 10Hz – 100kHz	150			µV (rms)
		BW = 300Hz – 300kHz	100			

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see Electrical Charateristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO220 package must be derated at θ_{jA} = 50˚C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO263 surface-mount package must be derated at θ_{jA} = 60˚C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient. The devices in SOT223 package must be derated at θ_{jA} = 90˚C/W (with 0.5in^2, 1oz. copper area), junction-to-ambient.

Note 3: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Note 4: Typical numbers are at 25˚C and represent the most likely parametric norm.

Note 5: Limits are 100% production tested at 25˚C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 6: If used in a dual-supply system where the regulator load is returned to a negative supply, the LP396X output must be diode-clamped to ground.

Note 7: The output PMOS structure contains a diode between the V_{IN} and V_{OUT} terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200mA of DC current and 1Amp of peak current.

Note 8: Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.

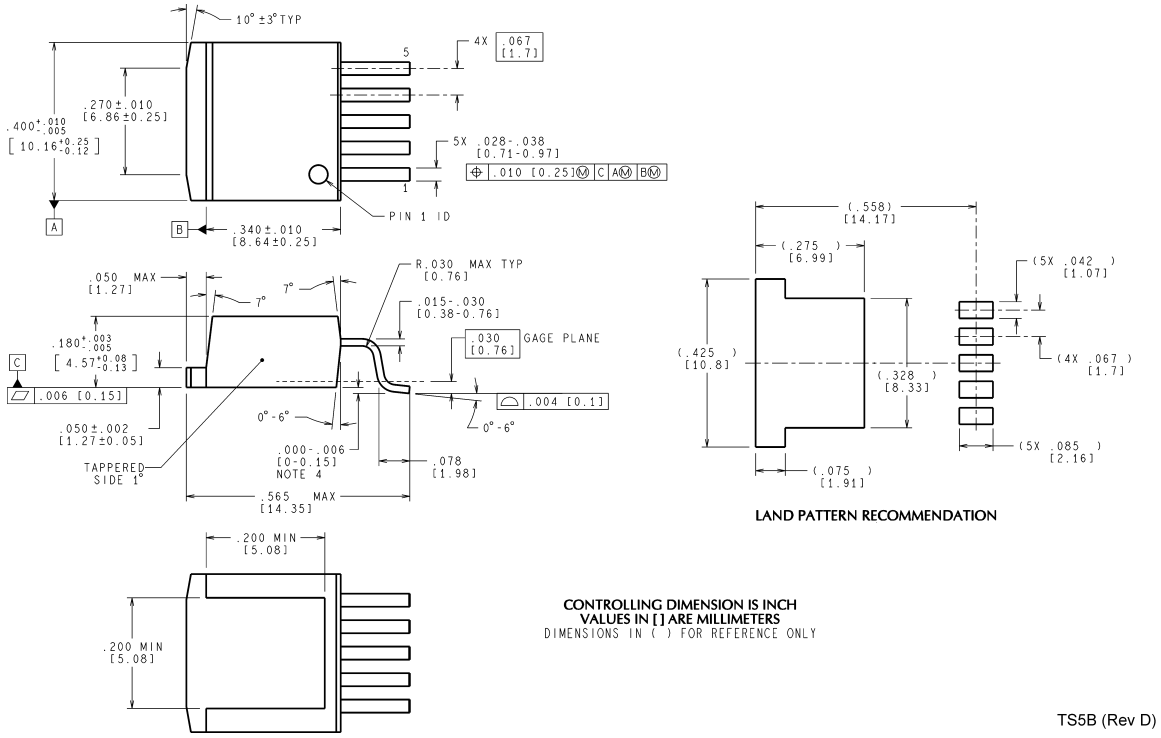
Note 9: $\overline{Error}$ Flag threshold and hysteresis are specified as percentage of regulated output voltage.

Note 10: Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5V.

Note 11: This specification has been tested for –40˚C ≤ T_J ≤ 85˚C since the temperature rise of the device is negligible under shutdown conditions.

Note 12: The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5V, whichever is greater.

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TS5B (Rev D)

TO263 5-Lead, Molded, Surface Mount Package (TO263-5)
NS Package Number TS5B
For Order Numbers, refer to the "Ordering Information" section of this document.