Microprocessor CORE Voltage Regulator Multi-Phase Buck PWM Controller

The HIP6301V and HIP6302V control microprocessor CORE voltage regulation by driving up to four synchronous-rectified buck channels in parallel. Multiphase buck converter architecture uses interleaved timing to multiply ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and a smaller implementation area. The HIP6301V is a versatile 2- to 4-phase controller and the HIP6302V is a cost-saving dedicated 2-phase controller.

The HIP6301V and HIP6302V are exact pin compatible replacements for their predecessor parts, the HIP6301 and HIP6302. They are the first controllers to incorporate Dynamic VID™ technology to manage the output voltage and current during on-the-fly DAC changes. Using Dynamic VID, the HIP6301V and HIP6302V detect changes in the VID code, and gradually change the reference in 25mV increments until reaching the new value. By gradually changing the reference setting, in-rush current and the accompanying voltage swings remain negligibly small.

Intersil offers a wide range of MOSFET drivers to form highly integrated solutions for high-current, high slew-rate applications. The HIP6301V and HIP6302V regulate output voltage, balance load currents and provide protective functions for two to four synchronous-rectified buck converter channels. These parts feature an integrated high-bandwidth error amplifier for fast, precise regulation and a 5-bit DAC for the digital interface to program the 0.8% accuracy. A window comparator toggles PGOOD if the output voltage moves out of range, and acts to protect the load in case of over voltage.

Current sensing is accomplished by reading the voltage developed across the lower MOSFETs during their conduction intervals. Current sensing provides the needed signals for precision droop, channel-current balancing, load sharing, and overcurrent protection. This saves cost by taking advantage of the power device's parasitic on resistance.

Features

- Multi-Phase Power Conversion
- Precision CORE Voltage Regulation
  - ±0.8% System Accuracy Over-Temperature
- Microprocessor Voltage Identification Input
  - Dynamic-VID Technology
  - 5-bit VID Decoder
- Precision Channel-Current Balance
- Overcurrent Protection
- Lossless Current Sensing
- Programmable "Droop" Voltage
- Fast Transient Response
- Selection of 2-, 3-, or 4-Phase Operation
- High Ripple Frequency (100kHz to 6MHz)
- Pb-Free Available (RoHS Compliant)

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP6301VCB*	HIP6301VCB	0 to +70	20 Ld SOIC	M20.3
HIP6301VCBZ* (Note)	HIP6301VCBZ	0 to +70	20 Ld SOIC (Pb-free)	M20.3
HIP6301VCBZA* (Note)	HIP6301VCBZ	0 to +70	20 Ld SOIC (Pb-free)	M20.3
HIP6302VCB*	HIP6302VCB	0 to +70	16 Ld SOIC	M16.15
HIP6302VCBZ* (Note)	HIP6302VCBZ	0 to +70	16 Ld SOIC (Pb-free)	M16.15

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +7V
Input, Output, or I/O Voltage . . . . . GND -0.3V to V_{CC} + 0.3V

Recommended Operating Conditions

Supply Voltage . . . . . +5V ±5%
Ambient Temperature . . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
16 Ld SOIC Package	70
20 Ld SOIC Package	65

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty..

NOTES:

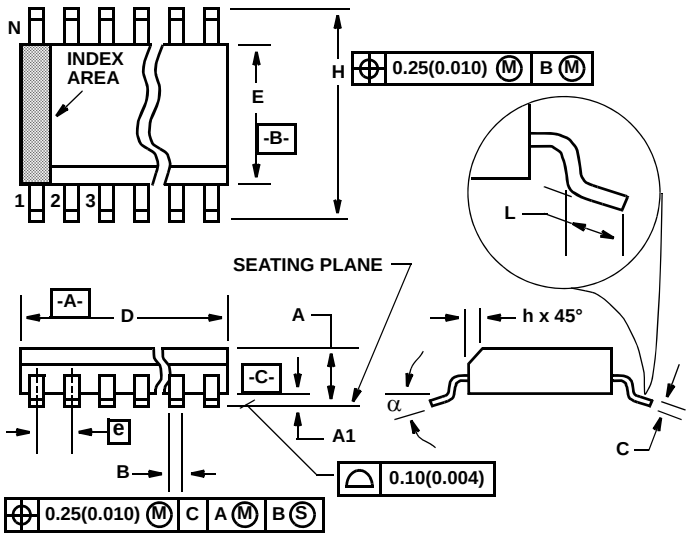
1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. (See Tech Brief TB379 for details.)
2. VID input levels above 2.9V may produce an reference-voltage offset inaccuracy.
3. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, T_A = +0°C to +70°C, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
INPUT SUPPLY POWER					
Input Supply Current	R_T = 100kΩ	-	-	15	mA
POR (Power-On Reset) Threshold	V_{CC} Rising	4.25	4.38	4.5	V
	V_{CC} Falling	3.75	3.88	4.00	V
REFERENCE AND DAC					
System Accuracy	Percent system deviation from programmed VID Codes	-0.8	-	0.8	%
DAC (VID0 - VID3) Input Low Voltage	DAC Programming Input Low Threshold Voltage	-	-	0.8	V
DAC (VID0 - VID3) Input High Voltage	DAC Programming Input High Threshold Voltage	2.0	-	-	V
VID Pull-Up	VIDx = 0V or VIDx = 2.5V (Note 2); Not tested - for reference only	10	-	40	µA
CHANNEL GENERATOR					
Frequency, F_{SW}	R_T = 100kΩ, ±1%	224	280	336	kHz
Disable Voltage	$V_{FS/DIS}$ to disable controller; Not tested - for reference, only	-	-	1.0	V
ERROR AMPLIFIER					
DC Gain	R_L = 10k to ground	-	72	-	dB
Gain-Bandwidth Product	C_L = 100pF, R_L = 10k to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, R_L = 10k to ground	-	5.3	-	V/µs
Maximum Output Voltage	R_L = 10k to ground	3.6	-	-	V
Minimum Output Voltage	R_L = 10k to ground	-	-	0.5	V
I_{SEN}					
Full-Scale Current Level	Not tested - for reference, only	-	50	-	µA
Overcurrent Trip Level	Not tested - for reference, only	-	82.5	-	µA
POWER-GOOD MONITOR					
Undervoltage Threshold	VSEN Rising	-	0.92	-	V_{DAC}
Undervoltage Threshold	VSEN Falling	-	0.90	-	V_{DAC}
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	-	0.4	V
PROTECTION					
Overvoltage Threshold	VSEN Rising	1.12	1.15	1.20	V_{DAC}
Overvoltage Hysteresis	VSEN Falling; Not tested - for reference, only	-	2	-	%

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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