Microprocessor CORE Voltage Regulator Multi-Phase Buck PWM Controller

The HIP6301 multi-phase PWM control IC together with its companion gate drivers, the HIP6601B, HIP6602B, HIP6603B or HIP6604B and external MOSFETs provides a precision voltage regulation system for advanced microprocessors. Multiphase power conversion is a marked departure from earlier single phase converter configurations previously employed to satisfy the ever increasing current demands of modern microprocessors. Multi-phase convertors, by distributing the power and load current results in smaller and lower cost transistors with fewer input and output capacitors. These reductions accrue from the higher effective conversion frequency with higher frequency ripple current due to the phase interleaving process of this topology. For example, a three phase convertor operating at 350kHz will have a ripple frequency of 1.05MHz. Moreover, greater convertor bandwidth of this design results in faster response to load transients.

Outstanding features of this controller IC include programmable VID codes from the microprocessor that range from 1.100V to 1.850V with a system accuracy of ±1%. Pull up currents on these VID pins eliminates the need for external pull up resistors. In addition “droop” compensation, used to reduce the overshoot or undershoot of the CORE voltage, is easily programmed with a single resistor.

Another feature of this controller IC is the PGOOD monitor circuit which is held low until the CORE voltage increases, during its Soft-Start sequence, to within 10% of the programmed voltage. Overvoltage, 15% above programmed CORE voltage, results in the converter shutting down and turning the lower MOSFETs ON to clamp and protect the microprocessor. Under voltage is also detected and results in PGOOD low if the CORE voltage falls 10% below the programmed level. Overcurrent protection reduces the regulator current to less than 25% of the programmed trip value. These features provide monitoring and protection for the microprocessor and power system.

Features

- Multi-Phase Power Conversion
- Precision Channel Current Sharing
  - Loss Less Current Sampling - Uses $r_{DS(ON)}$
- Precision CORE Voltage Regulation
  - ±1% System Accuracy Over Temperature
- Microprocessor Voltage Identification Input
  - 5-Bit VID Input
  - 1.100V to 1.850V in 25mV Steps
  - Programmable “Droop” Voltage
- Fast Transient Recovery Time
- Over Current Protection
- Automatic Selection of 2, 3, or 4 Phase Operation
- High Ripple Frequency, (Channel Frequency) Times Number Channels . . . . . .100kHz to 6MHz
- Pb-Free Available (RoHS Compliant)

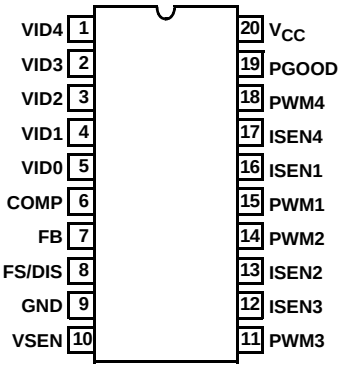
Ordering Information

PART NUMBER	TEMP. (°C)	PACKAGE	PKG. DWG #
HIP6301CB	0 to 70	20 Ld SOIC	M20.3
HIP6301CBZ (Note)	0 to 70	20 Ld SOIC (Pb-free)	M20.3
HIP6301CB-T	20 Ld SOIC Tape and Reel		
HIP6301CBZ-T (Note)	20 Ld SOIC Tape and Reel (Pb-free)		
HIP6301CBZA-T (Note)	20 Ld SOIC Tape and Reel (Pb-free)		
HIP6301EVAL2	Evaluation Platform		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

HIP6301 (SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +7V
Input, Output, or I/O Voltage . . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification 1.5kV

Recommended Operating Conditions

Supply Voltage . . . . . +5V ±5%
Ambient Temperature . . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	65

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, T_A = 0°C to 70°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY POWER					
Input Supply Current	R_T = 100kΩ	-	10	15	mA
	EN = 0V	4.25	8.8	4.5	mA
POR (Power-On Reset) Threshold	V_{CC} Rising	4.25	4.38	4.5	V
	V_{CC} Falling	3.75	3.88	4.00	V
REFERENCE AND DAC					
System Accuracy	Percent system deviation from programmed VID Codes	-1	-	1	%
DAC (VID0 - VID3) Input Low Voltage	DAC Programming Input Low Threshold Voltage	-	-	0.8	V
DAC (VID0 - VID3) Input High Voltage	DAC Programming Input High Threshold Voltage	2.0	-	-	V
VID Pull-Up	VIDx = 0V or VIDx = 3V	10	20	40	µA
CHANNEL GENERATOR, SAWTOOTH GENERATOR and Maximum PWM Duty Cycle					
Frequency, F_{SW}	R_T = 100kΩ, ±1%	224	280	336	kHz
Adjustment Range	See Figure 10	0.05	-	1.5	MHz
Disable Voltage	Maximum voltage at FS/DIS to disable controller. $I_{FS/DIS}$ = 1mA.	-	1.2	1.0	V
Sawtooth Amplitude	Amplitude of Sawtooh Generator at Channel Comparator Input	-	1.33	-	Vp-p
PWM Maximum Duty Cycle		-	75	-	%
ERROR AMPLIFIER					
DC Gain	R_L = 10K to ground	-	72	-	dB
Gain-Bandwidth Product	C_L = 100pF, R_L = 10K to ground	-	18	-	MHz
Slew Rate	C_L = 100pF, R_L = 10K to ground	-	5.3	-	V/µs
Maximum Output Voltage	R_L = 10K to ground	3.6	4.1	-	V
Minimum Output Voltage	R_L = 10K to ground	-	0.16	0.5	V
I_{SEN}					
Full Scale Input Current		-	50	-	µA
Overcurrent Trip Level		-67.5	-	-87.5	µA
POWER GOOD MONITOR					
Undervoltage Threshold	VSEN Rising	-	0.92	-	V_{DAC}
Undervoltage Threshold	VSEN Falling	-	0.90	-	V_{DAC}
PGOOD Low Output Voltage	I_{PGOOD} = 4mA	-	0.18	0.4	V

Electrical Specifications Operating Conditions: V_{CC} = 5V, T_A = 0°C to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PROTECTION					
Overvoltage Threshold	VSEN Rising	1.12	1.15	1.2	V_{DAC}
Percent Overvoltage Hysteresis	VSEN Falling after Overvoltage	-	2	-	%

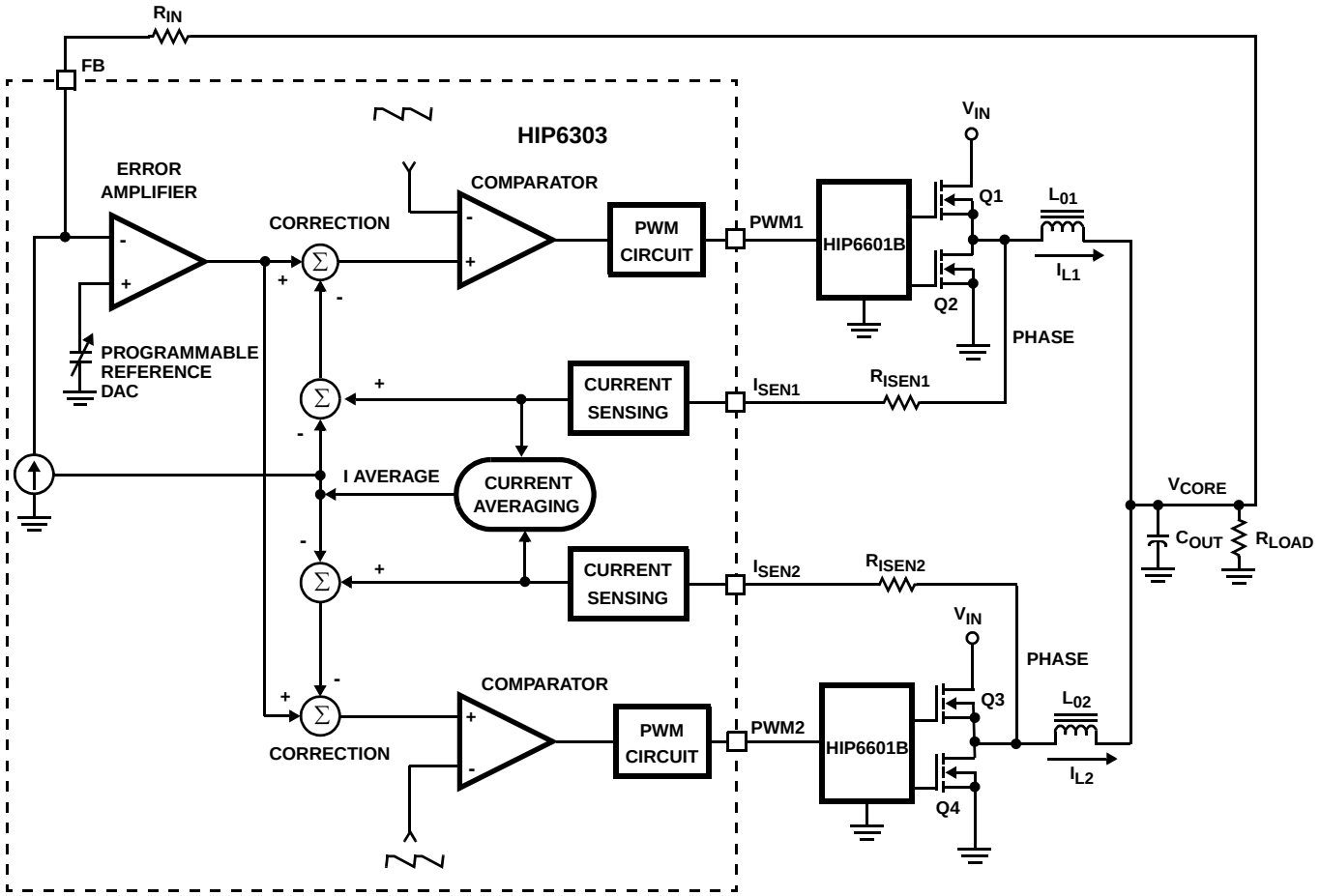


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THE HIP6301 VOLTAGE AND CURRENT CONTROL LOOPS FOR A TWO POWER CHANNEL REGULATOR

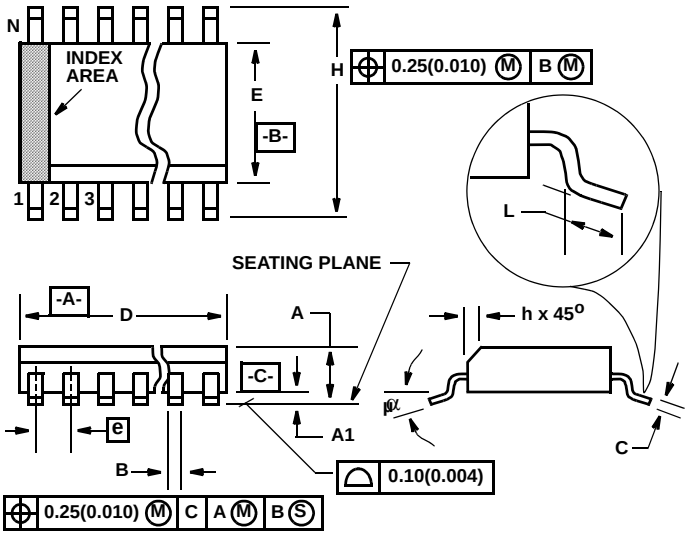
Operation

Figure 1 shows a simplified diagram of the voltage regulation and current control loops. Both voltage and current feedback are used to precisely regulate voltage and tightly control output currents, I_{L1} and I_{L2}, of the two power channels. The voltage loop comprises the Error Amplifier, Comparators, gate drivers and output MOSFETs. The Error Amplifier is essentially connected as a voltage follower that has as an input, the Programmable Reference DAC and an output that is the CORE voltage.

Voltage Loop

Feedback from the CORE voltage is applied via resistor R_{IN} to the inverting input of the Error Amplifier. This signal can drive the Error Amplifier output either high or low, depending upon the CORE voltage. Low CORE voltage makes the amplifier output move towards a higher output voltage level. Amplifier output voltage is applied to the positive inputs of the Comparators via the Correction summing networks. Out-of-phase sawtooth signals are applied to the two Comparators inverting inputs. Increasing Error Amplifier voltage results in increased Comparator output duty cycle. This increased duty cycle signal is passed through the PWM CIRCUIT with no phase reversal and on to the HIP6601B, again with no phase reversal for gate drive to the upper MOSFETs, Q1 and Q3. Increased duty cycle or ON time for the MOSFET transistors results in increased output voltage to compensate for the low output voltage sensed.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.014	0.019	0.35	0.49	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.