Data Sheet FN2855.4

Precision Quad Comparators

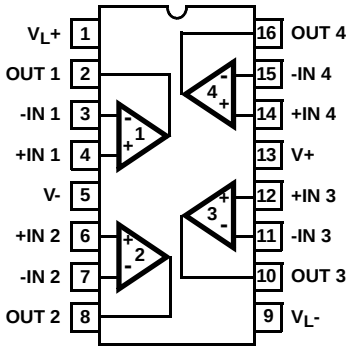
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{LOGIC}+ and V_{LOGIC}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features make them ideal components for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

For military grade product, refer to the HA-4902/883 data sheet.

Pinout

HA-4900, HA-4902 (CERDIP)
HA-4905 (PDIP, CERDIP, SOIC)
TOP VIEW



Features

- Fast Response Time 130ns
- Low Offset Voltage 2.0mV
- Low Offset Current 10nA
- Single or Dual Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit. No External Resistors Required
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Threshold Detector
- Zero Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (^{O}C)	PACKAGE	PKG. DWG. #
HA1-4900-2	HA1-4900-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-4902-2	HA1-4902-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-4905-5	HA1-4905-5	0 to 75	16 Ld CERDIP	F16.3
HA3-4905-5	HA3-4905-5	0 to 75	16 Ld PDIP	E16.3
HA9P4905-5	HA9P4905-5	0 to 75	16 Ld SOIC	M16.3
HA9P4905-5Z (See Note)	HA9P4905-5Z	0 to 75	16 Ld SOIC (Pb-free)	M16.3

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 33V
Differential Input Voltage 15V
Voltage Between V_{LOGIC}+ and V_{LOGIC}- 18V
Output Current 50mA
Power Dissipation (Notes 1, 2)

Operating Conditions

Temperature Range
HA-4900-2, HA-4902-2. . . . . -55^{o}C to 125^{o}C
HA-4905-5 . . . . . 0^{o}C to 75^{o}C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
CERDIP Package	85	25
PDIP Package	90	N/A
SOIC Package	100	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . .175^{o}C
Maximum Junction Temperature (Plastic Package) . . . . . .150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Die Characteristics

Back Side Potential . . . . . V-
Number of Transistors 137
Die Size . . . . . 95 mils x 105 mils

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below 175^{o}C for ceramic packages, and below 150^{o}C for plastic packages.
2. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{LOGIC} shown in curves of Power Dissipation vs Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{LOGIC}+, V_{LOGIC}-) gives a T.P.D. of 350mW, the combination +15V, -15V, +15V, 0V gives a T.P.D. of 450mW.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{SUPPLY} = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = GND

PARAMETER	TEMP (^{o}C)	HA-4900-2 -55^{o}C to 125^{o}C			HA-4902-2 -55^{o}C to 125^{o}C			HA-4905-5 0^{o}C to 75^{o}C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 4)	25	-	2	3	-	2	5	-	4	7.5	mV
	Full	-	-	4	-	-	8	-	-	10	mV
Offset Current	25	-	10	25	-	10	35	-	25	50	nA
	Full	-	-	35	-	-	45	-	-	70	nA
Bias Current (Note 5)	25	-	50	75	-	50	150	-	100	150	nA
	Full	-	-	150	-	-	200	-	-	300	nA
Input Sensitivity (Note 6)	25	-	-	V_{IO} + 0.3	-	-	V_{IO} + 0.5	-	-	V_{IO} + 0.5	mV
	Full	-	-	V_{IO} + 0.4	-	-	V_{IO} + 0.6	-	-	V_{IO} + 0.7	mV
Common Mode Range	Full	V-	-	(V+) - 2.4	V-	-	(V+) - 2.6	V-	-	(V+) - 2.4	V
Differential Input Resistance	25	-	250	-	-	250	-	-	250	-	MΩ
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25	-	400	-	-	400	-	-	400	-	kV/V
Response Time (t_{PD}(0)) (Note 7)	25	-	130	200	-	130	200	-	130	200	ns
Response Time (t_{PD}(1)) (Note 7)	25	-	180	215	-	180	215	-	180	215	ns

Electrical Specifications V_{SUPPLY} = ±15V, V_{LOGIC}+ = 5V, V_{LOGIC}- = GND **(Continued)**

PARAMETER	TEMP (^{o}C)	HA-4900-2 -55^{o}C to 125^{o}C			HA-4902-2 -55^{o}C to 125^{o}C			HA-4905-5 0^{o}C to 75^{o}C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS											
Output Voltage Level											
Logic “Low State” (V_{OL}) (Note 8)	Full	-	0.2	0.4	-	0.2	0.4	-	0.2	0.4	V
Logic “High State” (V_{OH}) (Note 8)	Full	3.5	4.2	-	3.5	4.2	-	3.5	4.2	-	V
Output Current											
I_{SINK}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
I_{SOURCE}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{PS} (+)	25	-	6.5	20	-	6.5	20	-	7	20	mA
Supply Current, I_{PS} (-)	25	-	4	8	-	4	8	-	5	8	mA
Supply Current, I_{PS} (Logic)	25	-	3.5	4	-	3.5	4	-	3.5	4	mA
Supply Voltage Range											
V_{LOGIC}+ (Note 2)	Full	0	-	+15.0	0	-	+15.0	0	-	+15.0	V
V_{LOGIC}- (Note 2)	Full	-15.0	-	0	-15.0	-	0	-15.0	-	0	V

NOTES:

4. Minimum differential input voltage required to ensure a defined output state.
5. Input bias currents are essentially constant with differential input voltages up to ±9V. With differential input voltages from ±9V to ±15V, bias current on the more negative input can rise to approximately 500µA. This will also cause higher supply currents.
6. V_{CM} = 0V. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage and voltage gain.
7. For $t_{PD}(1)$; 100mV input step, -10mV overdrive. For $t_{PD}(0)$; -100mV input step, 10mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Figure 1 for Test Circuit. All unused inverting inputs tied to +5V.
8. For V_{OH} and V_{OL}: I_{SINK} = I_{SOURCE} = 3.0mA. For other values of V_{LOGIC}; V_{OH} (Min) = V_{LOGIC} + -1.5V.

Test Circuit and Waveform

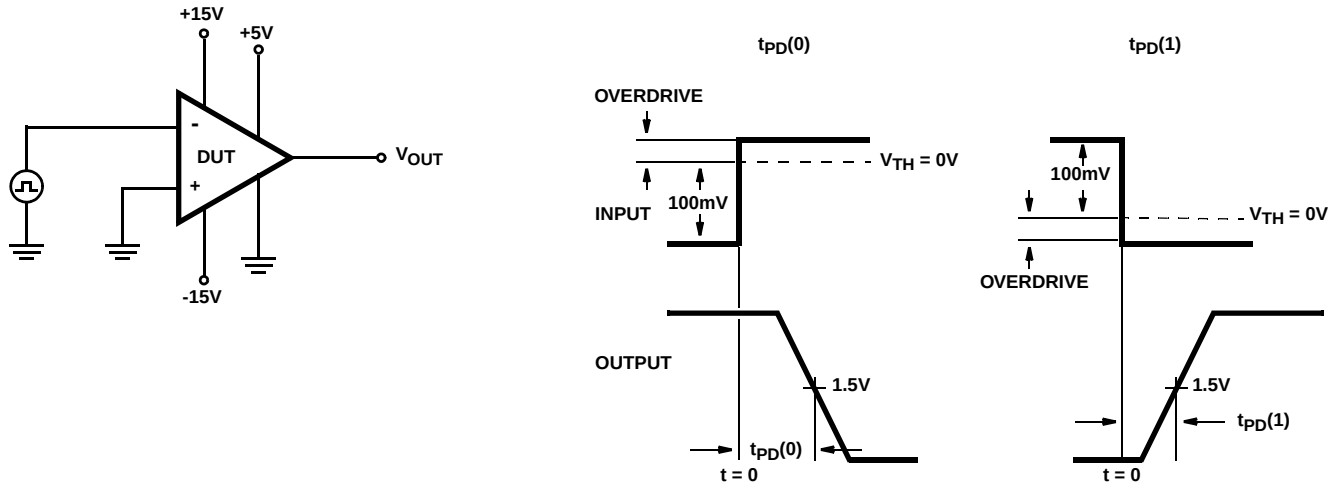


FIGURE 1.