CMOS Programmable Peripheral Interface

The Intersil 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Intersil advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Features

- Pb-Free Plus Anneal Available (RoHS Compliant) (See Ordering Info)
- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No “Wait State” Operation with 5MHz and 8MHz 80C86 and 80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- L7 Process
- 2.5mA Drive Capability on All I/O Ports
- Low Standby Power (ICCSB) 10µA

Ordering Information

PART NUMBERS				TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
5MHz	PART MARKING	8MHz	PART MARKING			
CP82C55A-5	CP82C55A-5	CP82C55A	CP82C55A	0 to +70	40 Ld PDIP	E40.6
CP82C55A-5Z (Note)	CP82C55A-5Z	CP82C55AZ (Note)	CP82C55AZ	0 to +70	40 Ld PDIP (Pb-free)	
		IP82C55A	IP82C55A	-40 to +85	40 Ld PDIP	
		IP82C55AZ (Note)	IP82C55AZ	-40 to +85	40 Ld PDIP (Pb-free)	
CS82C55A-5*	CS82C55A-5	CS82C55A*	CS82C55A*	0 to +70	44 Ld PLCC	N44.65
CS82C55A-5Z* (Note)	CS82C55A-5Z	CS82C55AZ* (Note)	CS82C55AZ	0 to +70	44 Ld PLCC (Pb-free)	
IS82C55A-5*	IS82C55A-5	IS82C55A*	IS82C55A*	-40 to +85	44 Ld PLCC	
IS82C55A-5Z* (Note)	IS82C55A-5Z	IS82C55AZ* (Note)	IS82C55AZ	-40 to +85	44 Ld PLCC (Pb-free)	
		CQ82C55A*	CQ82C55A*	0 to +70	44 Ld MQFP	Q44.10x10
		CQ82C55AZ (Note)	CQ82C55AZ	0 to +70	44 Ld MQFP (Pb-free)	
		IQ82C55A*	IQ82C55A*	-40 to +85	44 Ld MQFP	
		IQ82C55AZ* (Note)	IQ82C55AZ	-40 to +85	44 Ld MQFP (Pb-free)	
		ID82C55A	ID82C55A	-40 to +85	40 Ld CERDIP	F40.6
		MD82C55A/B	MD82C55A/B	-55 to +125		
		8406602QA	8406602QA	SMD#		
		8406602XA	8406602XA	SMD#	44 Ld CLCC	J44.A

*Add “96” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings T_A = +25°C

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC}+0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Voltage Range . . . . . +4.5V to 5.5V
Operating Temperature Range
CX82C55A . . . . . 0°C to 70°C
IX82C55A . . . . . -40°C to 85°C
MX82C55A . . . . . -55°C to 125°C

Die Characteristics

Gate Count. . . . . 1000 Gates

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC}(°C/W)
CERDIP Package	50	10
CLCC Package	65	14
PDIP Package	50	N/A
PLCC Package	55	N/A
MQFP Package	62	N/A

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature
CDIP Packages . . . . . +175°C
PDIP Packages . . . . . +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(PLCC and MQFP Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{CC} = 5.0V ±10%; T_A = Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
V_{IH}	Logical One Input Voltage		2.0 2.2	-	V
V_{IL}	Logical Zero Input Voltage		-	0.8	V
V_{OH}	Logical One Output Voltage	I_{OH} = -2.5mA, I_{OH} = -100µA	3.0 V_{CC} -0.4	-	V
V_{OL}	Logical Zero Output Voltage	I_{OL} +2.5mA	-	0.4	V
I_I	Input Leakage Current	V_{IN} = V_{CC} or GND, $\overline{RD}$, $\overline{CS}$, A1, A0, RESET, WR	-1.0	+1.0	µA
IO	I/O Pin Leakage Current	VO = V_{CC} or GND, D0 - D7	-10	+10	µA
IBHH	Bus Hold High Current	VO = 3.0V. Ports A, B, C			
		T_A = -55°C	-50	-450	µA
		T_A = +128°C	-50	-400	µA
IBHL	Bus Hold Low Current	VO = 1.0V. Port A ONLY			
		T_A = -55°C	50	450	µA
		T_A = +128°C	50	400	µA
IDAR	Darlington Drive Current	Ports A, B, C. Test Condition 3	-2.5	Note 2, 4	mA
ICCSB	Standby Power Supply Current	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND. Output Open	-	10	µA
ICCOP	Operating Power Supply Current	T_A = +25°C, V_{CC} = 5.0V, Typical (See Note 3)	-	1	mA/MHz

NOTES:

2. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
3. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0µs I/O Read/Write cycle time = 1mA).
4. Tested as V_{OH} at -2.5mA.

Capacitance T_A = +25°C

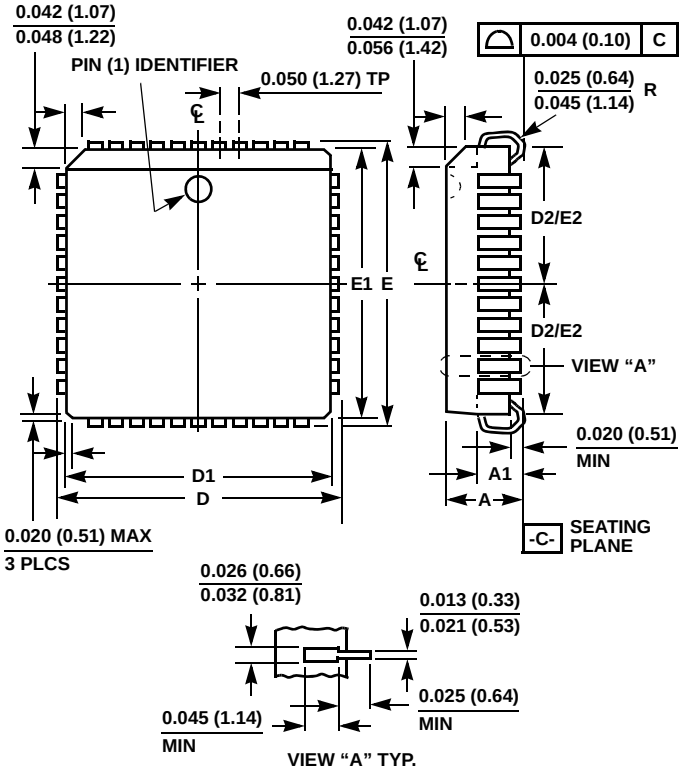
SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	10	pF	FREQ = 1MHz, All Measurements are referenced to device GND
CI/O	I/O Capacitance	20	pF	

AC Electrical Specifications V_{CC} = +5V± 10%, GND = 0V; T_A = Operating Temperature Range

SYMBOL	PARAMETER	82C55A-5		82C55A		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
READ TIMING							
(1) tAR	Address Stable Before $\overline{RD}$	0	-	0	-	ns	
(2) tRA	Address Stable After $\overline{RD}$	0	-	0	-	ns	
(3) tRR	$\overline{RD}$ Pulse Width	250	-	150	-	ns	
(4) tRD	Data Valid From $\overline{RD}$	-	200	-	120	ns	1
(5) tDF	Data Float After $\overline{RD}$	10	75	10	75	ns	2
(6) tRV	Time Between $\overline{RD}$s and/or $\overline{WR}$s	300	-	300	-	ns	
WRITE TIMING							
(7) tAW	Address Stable Before $\overline{WR}$	0	-	0	-	ns	
(8) tWA	Address Stable After $\overline{WR}$	20	-	20	-	ns	
(9) tWW	$\overline{WR}$ Pulse Width	100	-	100	-	ns	
(10) tDW	Data Valid to $\overline{WR}$ High	100	-	100	-	ns	
(11) tWD	Data Valid After $\overline{WR}$ High	30	-	30	-	ns	
OTHER TIMING							
(12) tWB	$\overline{WR}$ = 1 to Output	-	350	-	350	ns	1
(13) tIR	Peripheral Data Before $\overline{RD}$	0	-	0	-	ns	
(14) tHR	Peripheral Data After $\overline{RD}$	0	-	0	-	ns	
(15) tAK	ACK Pulse Width	200	-	200	-	ns	
(16) tST	STB Pulse Width	100	-	100	-	ns	
(17) tPS	Peripheral Data Before STB High	20	-	20	-	ns	
(18) tPH	Peripheral Data After STB High	50	-	50	-	ns	
(19) tAD	ACK = 0 to Output	-	175	-	175	ns	1
(20) tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
(21) tWOB	$\overline{WR}$ = 1 to OBF = 0	-	150	-	150	ns	1
(22) tAOB	ACK = 0 to OBF = 1	-	150	-	150	ns	1
(23) tSIB	STB = 0 to IBF = 1	-	150	-	150	ns	1
(24) tRIB	$\overline{RD}$ = 1 to IBF = 0	-	150	-	150	ns	1
(25) tRIT	$\overline{RD}$ = 0 to INTR = 0	-	200	-	200	ns	1
(26) tSIT	STB = 1 to INTR = 1	-	150	-	150	ns	1
(27) tAIT	ACK = 1 to INTR = 1	-	150	-	150	ns	1
(28) tWIT	$\overline{WR}$ = 0 to INTR = 0	-	200	-	200	ns	1
(29) tRES	Reset Pulse Width	500	-	500	-	ns	1, (Note)

NOTE: Period of initial Reset pulse after power-on must be at least 50µsec. Subsequent Reset pulses may be 500ns minimum.

Plastic Leaded Chip Carrier Packages (PLCC)



N44.65 (JEDEC MS-018AC ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.