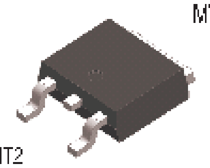
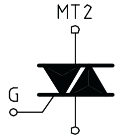
FAGOR

LOGIC LEVEL TRIAC

DPAK
(Plastic)





On-State Current
4 Amp

Gate Trigger Current
< 10 mA

Off-State Voltage
200 V ÷ 800 V

This series of TRIACs uses a high performance PNPN technology.

These parts are intended for general purpose AC switching applications with highly inductive loads.

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, T_C = 95 °C	4	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz (t = 16.7 ms)	33	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz (t = 20 ms)	30	A
I^2t	Fusing Current	t_p = 10 ms, Half Cycle	4.5	A^2s
I_{GM}	Peak Gate Current	20 µs max. T_j =125°C	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	T_j =125°C	1	W
dI/dt	Critical rate of rise of on-state current	I_G = 2x I_{GT}, $t_r \leq$ 100ns f= 120 Hz, T_j =125°C	50	A/µs
T_j	Operating Temperature		(-40 +125)	°C
T_{stg}	Storage Temperature		(-40 +150)	°C
T_{sld}	Soldering Temperature	10s max	260	°C

SYMBOL	PARAMETER	VOLTAGE					Unit
		B	D	M	S	N	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	200	400	600	700	800	V

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Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY 07	SENSITIVITY 08	Unit
I_{GT} (1)	Gate Trigger Current	V_D = 12 V_{DC} , R_L = 33Ω, T_j = 25 °C	Q1÷Q3 Q4	MAX MAX	5 7	10	mA mA
V_{GT}	Gate Trigger Voltage	V_D = 12 V_{DC} , R_L = 33Ω, T_j = 25 °C	Q1÷Q3 Q1÷Q4	MAX MAX	1.3 1.3		V V
V_{GD}	Gate Non Trigger Voltage	V_D = V_{DRM} , R_L = 3.3KΩ, T_j = 125 °C	Q1÷Q3 Q1÷Q4	MIN MIN	0.2 0.2		V V
I_H (2)	Holding Current	I_T = 100 mA , Gate open, T_j = 25 °C		MAX	15	15	mA
I_L	Latching Current	I_G = 1.2 I_{GT}, T_j = 25 °C	Q1, Q3 Q1,Q3,Q4 Q2	MAX MAX MAX	 20 30	25 30	mA mA mA
dV/dt (2)	Critical Rate of Voltage Rise	V_D = 0.67 x V_{DRM} , Gate open T_j = 125 °C		MIN	20	40	V/µs
(dI/dt)c (2)	Critical Rate of Current Rise	(dv/dt)c= 0.1 V/µs T_j = 125 °C (dv/dt)c= 10 V/µs T_j = 125 °C without snubber T_j = 125 °C		MIN MIN MIN	1.8 0.9 -	2.7 2.0 -	A/ms A/ms
V_{TM} (2)	On-state Voltage	I_T = 5.5 Amp, tp = 380 µs, T_j = 25 °C		MAX	1.6		V
$V_{t(o)}$ (2)	Threshold Voltage	T_j = 125 °C		MAX	0.9		V
r_d (2)	Dynamic Resistance	T_j = 125 °C		MAX	140		mΩ
I_{DRM}/I_{RRM}	Off-State Leakage Current	V_D = V_{DRM} , T_j = 125 °C V_R = V_{RRM} , T_j = 25 °C		MAX MAX	0.5 5		mA µA
$R_{th(j-c)}$	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.2		°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient	S = 1cm ^{2}			70		°C/W

(1) Minimum I_{GT} is guaranted at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

PART NUMBER INFORMATION

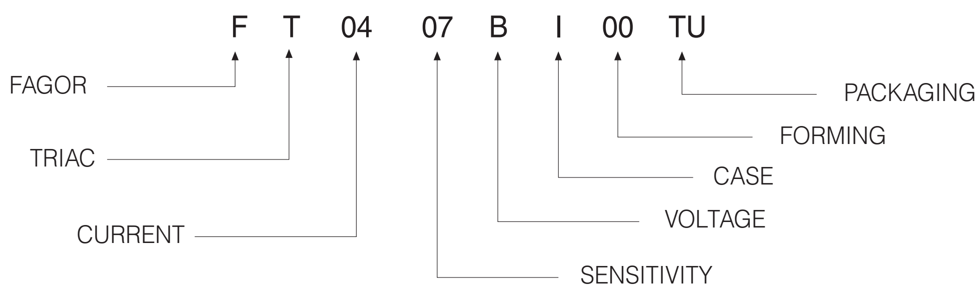

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Fig. 1: Maximum power dissipation versus RMS on-state curren (full cycle).

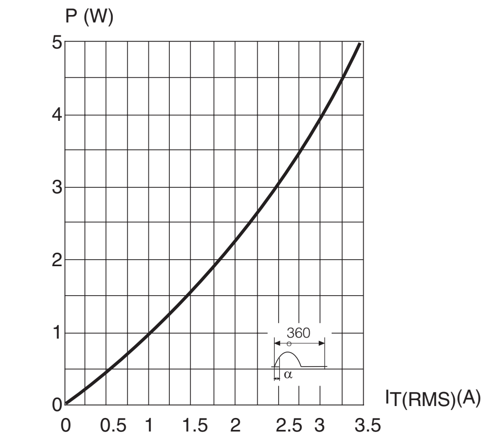

Fig. 2: RMS on-state current versus case temperature (full cycle).

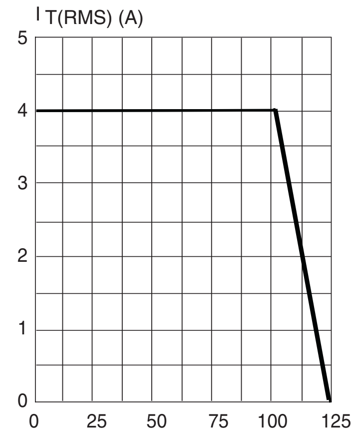

Fig. 3: : Relative variation of thermal impedance versus pulse duration.

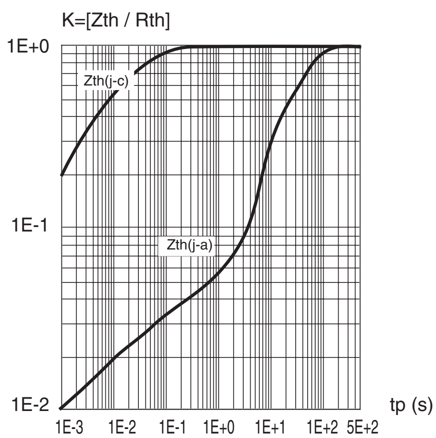

Fig. 4: On-state characteristics (maximum values)

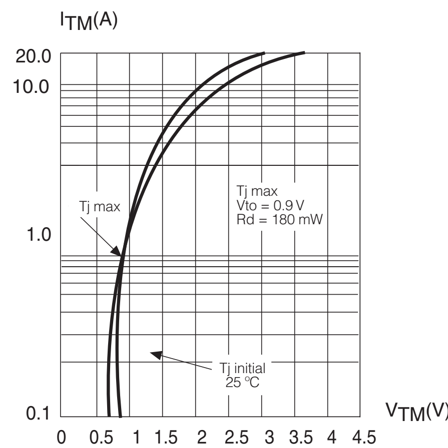

Fig. 5: Surge peak on-state current versus number of cycles

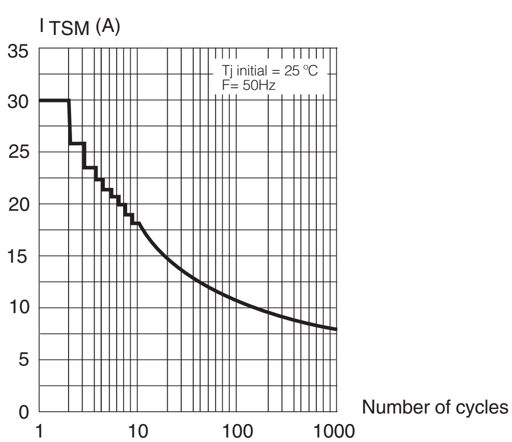

Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponding value of I^2t.

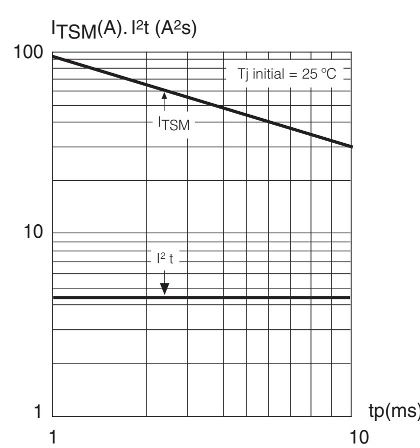

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Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

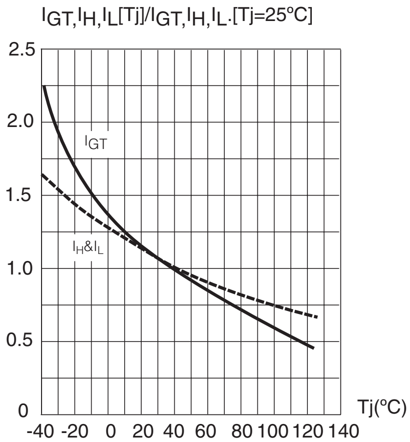


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

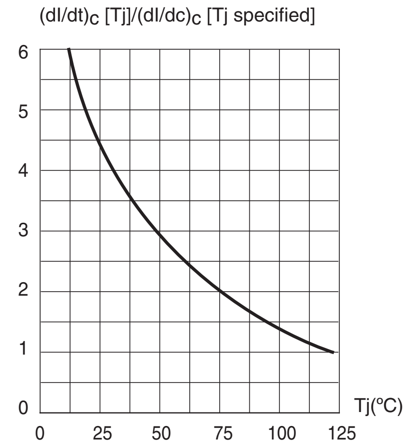
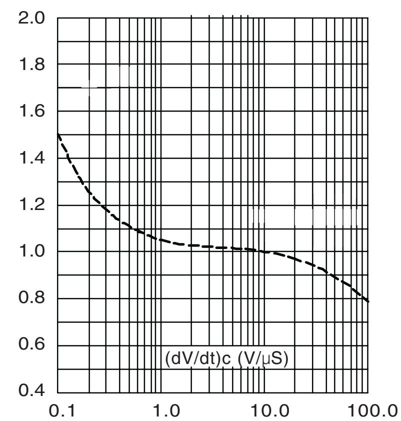


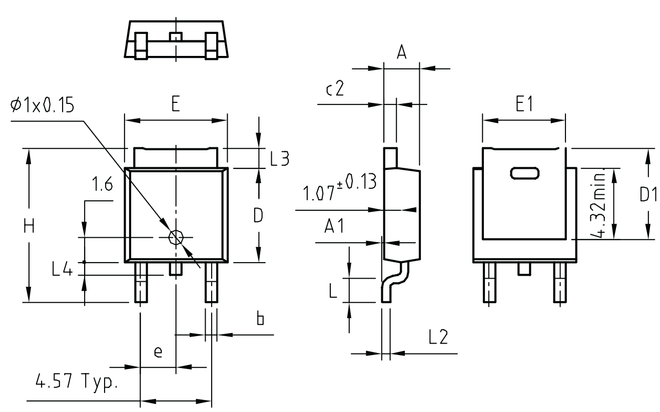
Fig. 9: Relative variation of critical rate of decrease of main current versus

(dV/dt)c (typical values).



PACKAGE MECHANICAL DATA

DPAK TO



REF	DIMENSIONS		
	Milimeters		
	Min.	Nominal	Max.
A			2.39
A1			0.127
b			0.89
c			0.61
c1			0.56
c2			
D			6.22
D1			5.52
E			6.73
E1			5.46
e			
H			10.41
L			1.78
L1			2.74
L2			0.58
L3			1.27
L4			1.02

Marking: type number
Weight: 0.2 g