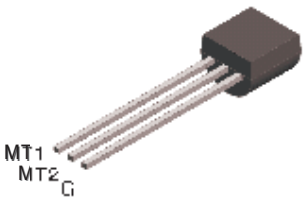
FAGOR

# LOGIC LEVEL TRIAC

TO92
(Plastic)





**On-State Current**
1 Amp

**Gate Trigger Current**
< 10 mA

**Off-State Voltage**
200 V ÷ 800 V (07, 09)
200 V ÷ 600 V (02, 03, 04, 05)

This series of TRIACs uses a high performance PNPN technology.

These parts are intended for general purpose AC switching applications with highly inductive loads.

## Absolute Maximum Ratings, according to IEC publication No. 134

| SYMBOL | PARAMETER | CONDITIONS | Value | Unit |
|---|---|---|---|---|
| $I_{T(RMS)}$ | RMS On-state Current (full sine wave) | All Conduction Angle, $T_C$ = 95 °C | 1 | A |
| $I_{TSM}$ | Non-repetitive On-State Current | Full Cycle, 60 Hz (t = 16.7 ms) | 8.5 | A |
| $I_{TSM}$ | Non-repetitive On-State Current | Full Cycle, 50 Hz (t = 20 ms) | 8 | A |
| $I^2t$ | Fusing Current | tp = 10 ms, Half Cycle | 0.32 | $A^2s$ |
| $I_{GM}$ | Peak Gate Current | 20 µs max. $T_j$ =125°C | 1 | A |
| $P_{G(AV)}$ | Average Gate Power Dissipation | $T_j$ =125°C | 0.1 | W |
| dI/dt | Critical rate of rise of on-state current | $I_G$ = 2x $I_{GT}$, tr ≤100ns<br>f= 120 Hz, $T_j$ =125°C | 20 | A/µs |
| $T_j$ | Operating Temperature | | (-40 +125) | °C |
| $T_{stg}$ | Storage Temperature | | (-40 +150) | °C |
| $T_{sld}$ | Soldering Temperature | 10s max | 260 | °C |

| SYMBOL | PARAMETER | VOLTAGE | | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | B | D | M | S * | N * | |
| $V_{DRM}$<br>$V_{RRM}$ | Repetitive Peak Off State Voltage | 200 | 400 | 600 | 700 | 800 | V |

* 07, 09 sensitivities

# LOGIC LEVEL TRIAC

## Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | Quadrant | | SENSITIVITY | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | 02 | 03 | 04 | 05 | 07 | 09 | |
| $I_{GT}$ (1) | Gate Trigger Current | $V_D$ = 12 $V_{DC}$ , $R_L$ = 33Ω, $T_j$ = 25 °C | Q1÷Q3 | MAX | 3 | 3 | 5 | 5 | 5 | 10 | mA |
| | | | Q4 | MAX | 3 | 5 | | 5 | 7 | 10 | mA |
| $V_{GT}$ | Gate Trigger Voltage | $V_D$ = 12 $V_{DC}$ , $R_L$ = 33Ω, $T_j$ = 25 °C | Q1÷Q3 | MAX | 1.3 | | | | | | V |
| | | | Q1÷Q4 | MAX | 1.3 | | | | | | V |
| $V_{GD}$ | Gate Non Trigger Voltage | $V_D$ = $V_{DRM}$ , $R_L$ = 3.3KΩ, $T_j$ = 125 °C | Q1÷Q3 | MIN | 0.2 | | | | | | V |
| | | | Q1÷Q4 | MIN | 0.2 | | | | | | V |
| $I_H$ (2) | Holding Current | $I_T$ = 100 mA , Gate open, $T_j$ = 25 °C | | MAX | 7 | 7 | 10 | 10 | 10 | 20 | mA |
| $I_L$ | Latching Current | $I_G$ = 1.2 $I_{GT}$, $T_j$ = 25 °C | Q1, Q3 | MAX | | | 10 | | | | mA |
| | | | Q1,Q3,Q4 | MAX | 7 | 7 | | 10 | 10 | 20 | mA |
| | | | Q2 | MAX | 15 | 20 | 20 | 20 | 20 | 25 | mA |
| dV/dt (2) | Critical Rate of Voltage Rise | $V_D$ = 0.67 x $V_{DRM}$ , Gate open $T_j$ = 125 °C | | MIN | 10 | 10 | 20 | 20 | 20 | 50 | V/µs |
| (dI/dt)c (2) | Critical Rate of Current Rise | (dv/dt)c= 0.1 V/µs $T_j$ = 125 °C | | MIN | 1.2 | 1.2 | 1.8 | 1.8 | 1.8 | 2.5 | A/ms |
| | | (dv/dt)c= 10 V/µs $T_j$ = 125 °C | | MIN | 0.6 | 0.6 | 0.9 | 0.9 | 0.9 | 1.5 | A/ms |
| | | without snubber $T_j$ = 125 °C | | MIN | | | | | | | |
| $V_{TM}$ (2) | On-state Voltage | $I_T$ = 1.1 Amp, tp = 380 µs, $T_j$ = 25 °C | | MAX | 1.95 | | | | | | V |
| $V_{t(o)}$ (2) | Threshold Voltage | $T_j$ = 125 °C | | MAX | 0.95 | | | | | | V |
| $r_d$ (2) | Dynamic Resistance | $T_j$ = 125 °C | | MAX | 1000 | | | | | | mΩ |
| $I_{DRM}/I_{RRM}$ | Off-State Leakage Current | $V_D$ = $V_{DRM}$ , $T_j$ = 125 °C | | MAX | 0.5 | | | | | | mA |
| | | $V_R$ = $V_{RRM}$ , $T_j$ = 25 °C | | MAX | 5 | | | | | | µA |
| $R_{th(j-c)}$ | Thermal Resistance Junction-Case | for AC 360° conduction angle | | | 80 | | | | | | °C/W |
| $R_{th(j-a)}$ | Thermal Resistance Junction-Ambient | S = 1 $cm^2$ | | | 150 | | | | | | °C/W |

(1) Minimum $I_{GT}$ is guaranted at 5% of $I_{GT}$ max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

## PART NUMBER INFORMATION

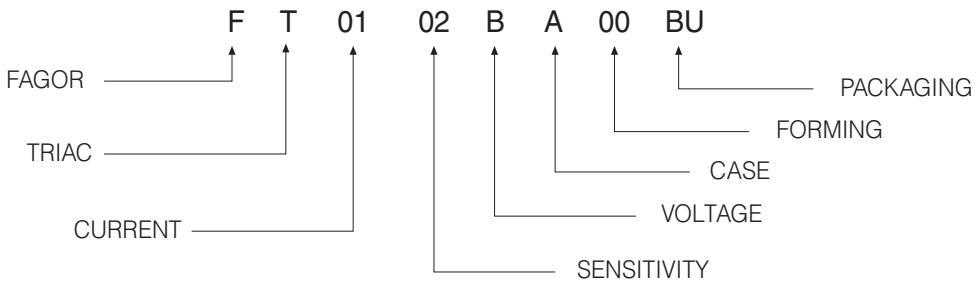


Fig. 1: Maximum power dissipation versus RMS on-state curren (full cycle).

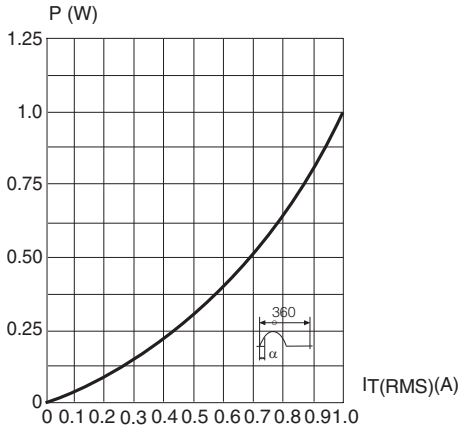



Fig. 2: RMS on-state current versus case temperature (full cycle).

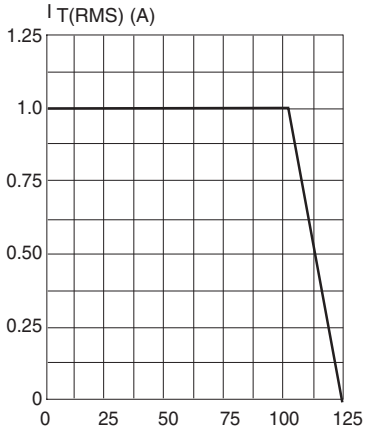



Fig. 3: : Relative variation of thermal impedance versus pulse duration.

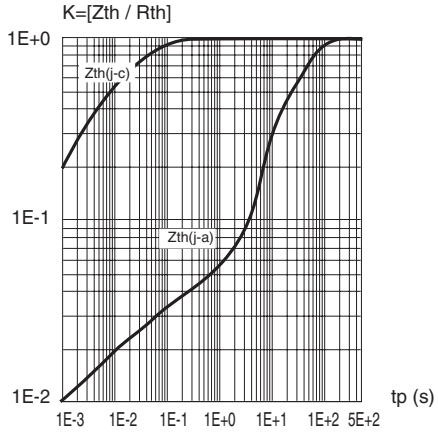



Fig. 4: On-state characteristics (maximum values)

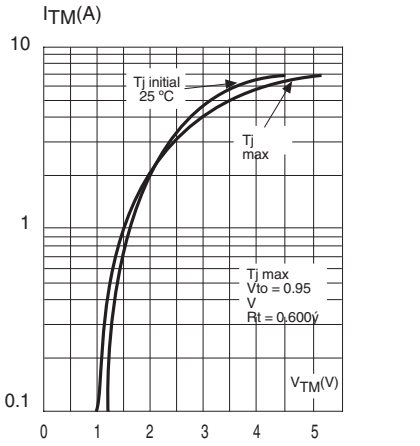



Fig. 5: Surge peak on-state current versus number of cycles

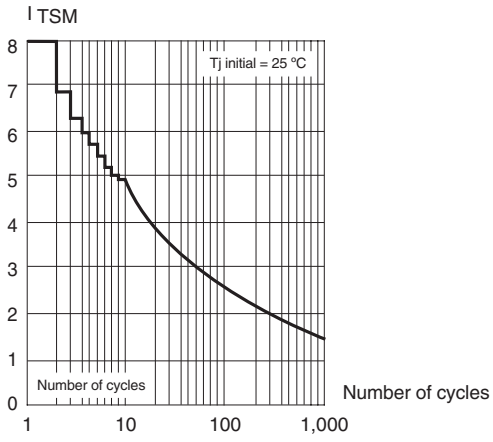



Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponding value of $I^2t$.

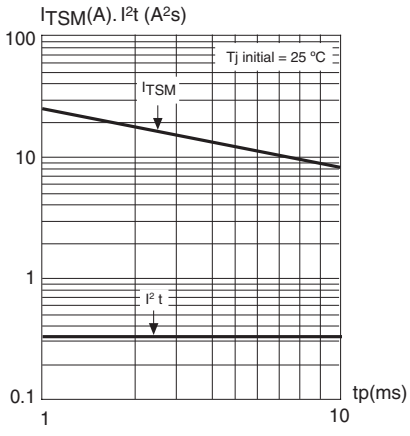


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Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

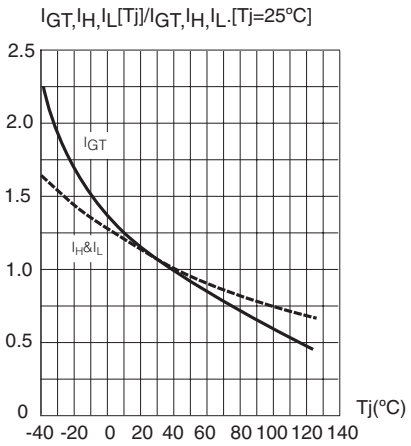



Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

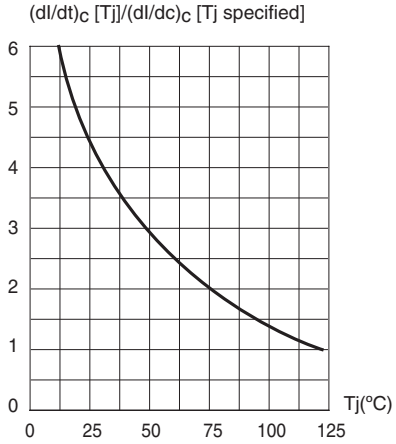
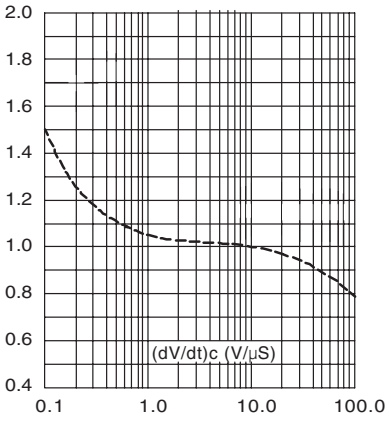
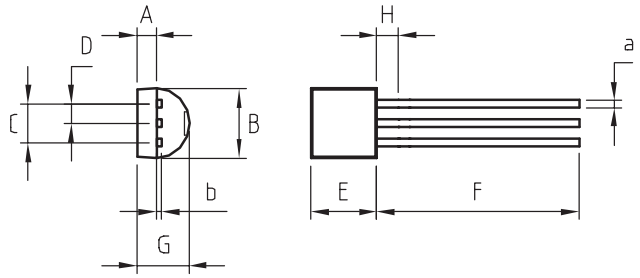



Fig. 9: Relative variation of critical rate of decrease of main current versus

(dV/dt)c (typical values).



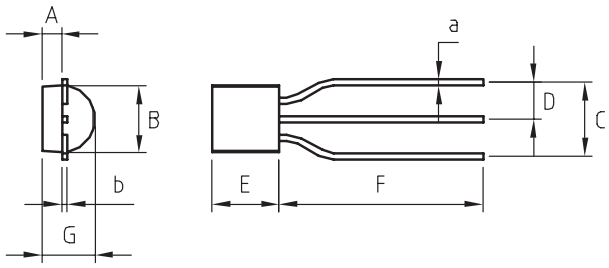

## PACKAGE MECHANICAL DATA TO92




| REF. | DIMENSIONS Milimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.9 | 1.2 | 1.5 |
| B | 4.40 | 4.6 | 4.80 |
| C | 2.34 | 2.54 | 2.74 |
| D | 1.07 | 1.27 | 1.47 |
| E | 4.40 | 4.6 | 4.80 |
| F | 12.7 | 14.1 | 15.5 |
| G | 3.40 | 3.6 | 3.86 |
| H | 1.30 | 1.5 | 1.70 |
| a | 0.38 | 0.44 | 0.51 |
| b | 0.33 | 0.41 | 0.51 |

Marking: type number
Weight: 0.2 g

## PACKAGE MECHANICAL DATA TO92 (FORTAPE & REEL)




| REF. | DIMENSIONS Milimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | - | 1.5 | - |
| B | 4.55 | 4.6 | 4.65 |
| C | 4.96 | 5.08 | 5.2 |
| D | 2.42 | 2.54 | 2.66 |
| E | 4.55 | 4.6 | 4.65 |
| F | 12.7 | 14.1 | 15.5 |
| G | 3.55 | 3.6 | 3.65 |
| a | 0.38 | 0.43 | 0.48 |
| b | 0.33 | 0.38 | 0.43 |

Marking: type number
Weight: 0.2 g