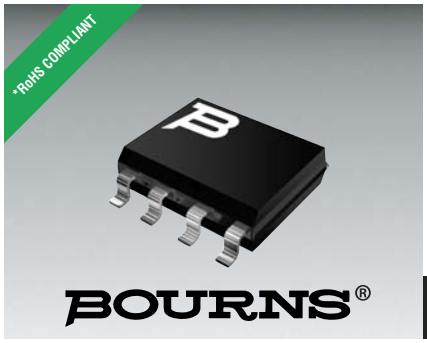
TISP6NTP2x - Quad Programmable Thyristor Surge Protector

Device Number	TISP6NTP2A	TISP6NTP2C
Package Options	DR	DR
Protection Voltage (V)	0 to -90	0 to -170
Ratings for Lightning Surge Standards - GR-1089-CORE 2/10 us (A)	85	90
Ratings for Lightning Surge Standards - GR-1089-CORE 2/10 us (A)	60	-
Ratings for Lightning Surge Standards - ANSI C62.41 8/20 us (A)	60	-
Ratings for Lightning Surge Standards - ITU-T K.20/45/21 5/310 us (A)	25	40
Ratings for Lightning Surge Standards - GR-1089-CORE 10/1000 us (A)	20	25

QUAD FORWARD-CONDUCTING BUFFERED P-GATE THYRISTORS



TISP6NTP2A Programmable Protector

Independent Overvoltage Protection for Two SLICs in Short Loop Applications:
– Wide 0 to -90 V Programming Range
– Low 5 mA max. Gate Triggering Current
– High 150 mA min. (85 °C) Holding Current
– Specified 1.2/50 & 0.5/700 Limiting Voltage
– Full -40 °C to 85 °C Temperature Range

Rated for Common Impulse Waveforms

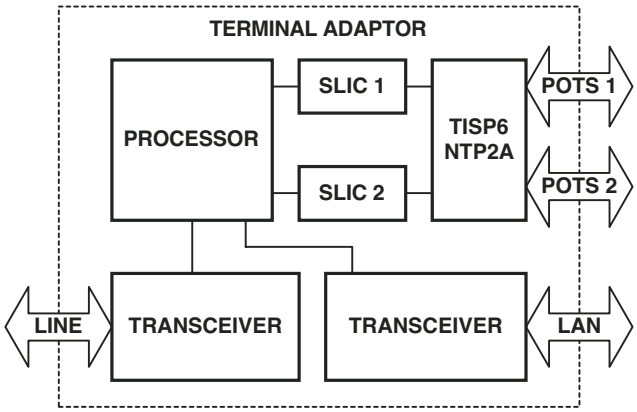
Voltage Impulse Form	Current Impulse Shape	I_{TSP} A
10/1000 µs	10/1000 µs	20
10/700 µs	5/310 µs	25
1.2/50 µs	8/20 µs	75
2/10 µs	2/10 µs	85

..... UL Recognized Component

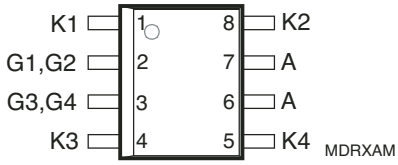
Description

The TISP6NTP2A has been designed for short loop systems such as:
– WILL (Wireless In the Local Loop)
– FITL (Fibre In The Loop)
– DAML (Digital Added Main Line, Pair Gain)
– SOHO (Small Office Home Office)
– ISDN-TA (Integrated Services Digital Network - Terminal Adaptors)

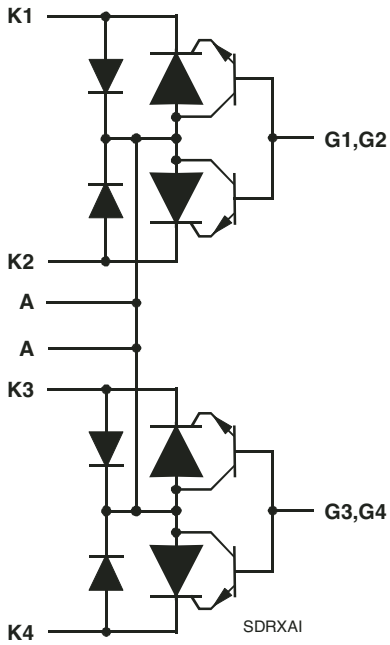
Typical TISP6NTP2A Router Application



D Package (Top View)



Device Symbol



How To Order

Device	Package	Carrier	Order As
TISP6NTP2A	D, Small-Outline	Tape and Reel	TISP6NTP2ADR-S

Description (continued)

These systems often have the need to source two POTS (Plain Old Telephone Service) lines, one for a telephone and the other for a facsimile machine. In a single surface mount package, the TISP6NTP2A protects the two POTS line SLICs (Subscriber Line Interface Circuits) against overvoltages caused by lightning, a.c. power contact and induction.

The TISP6NTP2A has an array of four buffered P-gate forward conducting thyristors with twin commoned gates and a common anode connection. Each thyristor cathode has a separate terminal connection. An antiparallel anode-cathode diode is connected across each thyristor. The buffer transistors reduce the gate supply current.

In use, the cathodes of an TISP6NTP2A thyristor are connected to the four conductors of two POTS lines (see applications information). Each gate is connected to the appropriate negative voltage battery feed of the SLIC driving that line pair. By having separate gates, each SLIC can be protected at a voltage level related to the negative supply voltage of that individual SLIC. The anode of the TISP6NTP2A is connected to the SLIC common.

Positive overvoltages are clipped to common by forward conduction of the TISP6NTP2A antiparallel diode. Negative overvoltages are initially clipped close to the SLIC negative supply by emitter follower action of the TISP6NTP2A buffer transistor. If sufficient clipping current flows, the TISP6NTP2A thyristor will regenerate and switch into a low voltage on-state condition. As the overvoltage subsides, the high holding current of the TISP6NTP2A prevents d.c. latchup.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, I_G = 0,- 40 °C ≤ T_J ≤ 85 °C	V_{DRM}	-100	V
Repetitive peak gate-cathode voltage, V_{KA} = 0,- 40 °C ≤ T_J ≤ 85 °C	V_{GKRM}	-90	V
Non-repetitive peak on-state pulse current, -40 °C ≤ T_J ≤ 85 °C, (see Notes 1 and 2)	I_{TSP}		A
10/1000 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)		20	
0.2/310 µs (I3124, open-circuit voltage wave shape 0.5/700 µs)		25	
5/310 µs (ITU-T K.20 & K.21, open-circuit voltage wave shape 10/700 µs)		25	
8/20 µs (IEC 61000-4-5:1995, open-circuit voltage wave shape 1.2/50 µs)		75	
2/10 µs (Bellcore GR-1089-CORE, Issue 1, November 1994, Section 4)		85	
Non-repetitive peak on-state current, 50/60 Hz, -40 °C ≤ T_J ≤ 85 °C, (see Notes 1 and 2)	I_{TSM}		A
100 ms		7	
1 s		2.7	
5 s		1.5	
300 s		0.45	
900 s		0.43	
Non-repetitive peak gate current, 1/2 µs pulse, cathodes commoned (see Note 1)	I_{GSM}	25	A
Operating free-air temperature range	T_A	-40 to +85	°C
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially, the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions.

2. These non-repetitive rated currents are peak values for either polarity. The rated current values may be applied to any cathode-anode terminal pair. Additionally, all cathode-anode terminal pairs may have their rated current values applied simultaneously (in this case the anode terminal current will be four times the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.

Recommended Operating Conditions

		Min.	Typ.	Max.	Unit
C_G	Gate decoupling capacitor	100	220		nF
R1, R2	Series resistor for GR-1089-CORE first-level surge survival Series resistor for ITU-T recommendation K.20 Series resistor for ITU-T recommendation K.21 Series resistor for IEC 61000-4-5:1995, class 5, 1.2/50 or 10/700	40 12 20 4			Ω

Electrical Characteristics for any Section, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
I_D	Off-state current	$V_D = V_{DRM}$, $I_G = 0$	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
$V_{(BO)}$	Breakover voltage	I_T = -20 A, IEC 61000-4-5:1995 combination impulse generator, V_{GG} = -50 V I_T = -18 A, I3124 impulse generator, V_{GG} = -50 V				-70 -70	V
$t_{(BR)}$	Breakdown time	I_T = -18 A, I3124 impulse generator, $V_{(BR)}$ < -50 V				2	μs
V_F	Forward voltage	I_F = 0.6 A, t_w = 500 μs, V_{GG} = -50 V I_F = 18 A, t_w = 500 μs, V_{GG} = -50 V				3 5	V
V_{FRM}	Peak forward recovery voltage	I_F = 20 A, IEC 61000-4-5:1995 combination impulse generator, V_{GG} = -50 V I_F = 18 A, I3124 impulse generator, V_{GG} = -50 V				15 15	V
t_{FR}	Forward recovery time	I_F = 18 A, I3124 impulse generator, V_{GG} = -50 V	V_F > 10 V V_F > 5 V			2 4	μs
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -50 V, T_J = 85 °C		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GKRM}$, V_{AK} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
I_{GAT}	Gate reverse current, on state	I_T = -0.6 A, t_w = 500 μs, V_{GG} = -50 V				-1	mA
I_{GAF}	Gate reverse current, forward conducting state	I_F = 0.6 A, t_w = 500 μs, V_{GG} = -50 V				-40	mA
I_{GT}	Gate trigger current	I_T = -5 A, $t_{p(g)}$ ≥ 20 μs, V_{GG} = -50 V				5	mA
V_{GT}	Gate trigger voltage	I_T = -5 A, $t_{p(g)}$ ≥ 20 μs, V_{GG} = -50 V				2.5	V
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 3)	V_D = -3 V			100	pF
			V_D = -50 V			60	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	P_{tot} = 0.52 W, T_A = 85 °C, 5 cm^2, FR4 PCB			160	°C/W