TISP6xxxx - Dual Programmable Thyristor Surge Protector

Device Number	TISP61089H	TISP61089B	TISP61089BS	TISP61089A	TISP61089AS
Package Options	DM	DR	DR	DR	DR
Protection Voltage (V)	0 to -155	0 to -170	0 to -170	0 to -120	0 to -120
Ratings for Lightning Surge Standards - GR-1089-CORE 2/10 us (A)	500	120	120	120	120
Ratings for Lightning Surge Standards - ANSI C62.41 8/20 us (A)	-	-	-	-	-
Ratings for Lightning Surge Standards - ITU-T K.20/45/21 5/310 us (A)	150	40	40	40	40
Ratings for Lightning Surge Standards - GR-1089-CORE 10/1000 us (A)	100	30	30	30	30

Device Number	TISP61089	TISP61089S	TISP61521	TISP61511
Package Options	DR	DR	DR	DR
Protection Voltage (V)	0 to -85	0 to -85	0 to -175	0 to -85
Ratings for Lightning Surge Standards - GR-1089-CORE 2/10 us (A)	120	120	170	170
Ratings for Lightning Surge Standards - ANSI C62.41 8/20 us (A)	-	-	100	90
Ratings for Lightning Surge Standards - ITU-T K.20/45/21 5/310 us (A)	40	40	40	40
Ratings for Lightning Surge Standards - GR-1089-CORE 10/1000 us (A)	30	30	30	30

TISP61089D, TISP61089SD, TISP61089AD, TISP61089ASD

DUAL FORWARD-CONDUCTING P-GATE THYRISTORS PROGRAMMABLE OVERVOLTAGE PROTECTORS

TISP61089 Gated Protector Series

Overvoltage Protection for Negative Rail SLICs

Dual Voltage-Tracking Protectors
- **'61089 for Battery Voltages to ..... -75 V**
- **'61089A for Battery Voltages to ..... -100 V**
- **Low Gate Triggering Current ..... < 5 mA**
- **High Holding Current ..... > 150 mA**

Rated for GR-1089-CORE and K.44 Impulses

Impulse Wave Shape		I_{PPSM}
Voltage	Current	A
2/10	2/10	120
10/700	5/310	40
10/1000	10/1000	30

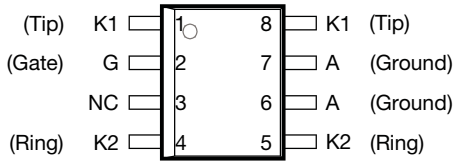
2/10 Overshoot Voltage Specified

Element	I_{PP} = 100 A, 2/10 V
Diode	8
SCR	12

Package Options
- **Surface Mount 8-pin Small-Outline**
  Line Feed-Thru Connection (D)
  Shunt Version Connection (SD)

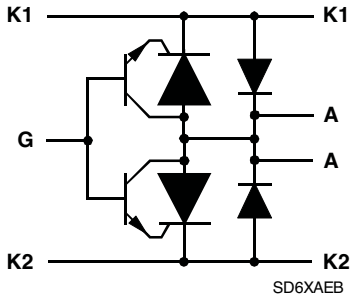
..... UL Recognized Components

D Package Top View and Device Symbol for Feed-Thru Pin-Out



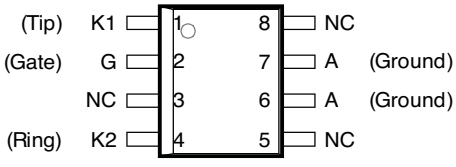
NC - No internal connection
Terminal typical application names shown in parenthesis

MD6XBDa



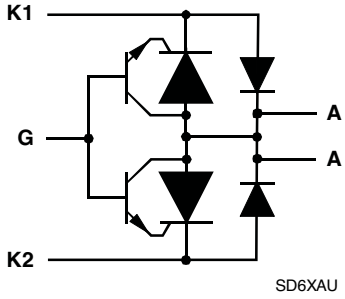
SD6XAEB

D Package Top View and Device Symbol for Shunt (SD) Pin-Out



MD6XBE

NC - No internal connection
Terminal typical application names shown in parenthesis



SD6XAU

How To Order

Device	Package	Carrier	Order As
TISP61089	D (Small-Outline)	R†	TISP61089DR-S
TISP61089S	D (Small-Outline)	R†	TISP61089SDR-S
† Carrier R is Embossed Tape Reeled			

Device	Package	Carrier	Order As
TISP61089A	D (Small-Outline)	R†	TISP61089ADR-S
TISP61089AS	D (Small-Outline)	R†	TISP61089ASDR-S
† Carrier R is Embossed Tape Reeled			

Description

These '61089 parts are all dual forward-conducting buffered p-gate thyristor (SCR) overvoltage protectors. They are designed to protect monolithic SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction. The '61089 limits voltages that exceed the SLIC supply rail voltage. The '61089 parameters are specified to allow equipment compliance with Telcordia (formally Bellcore) GR-1089-CORE and ITU-T recommendations K.20, K.21 and K.45.

The SLIC line driver section is typically powered from 0 V (ground) and a negative (battery) voltage. The protector gate is connected to this negative supply. This references the protection (clipping) voltage to the negative supply voltage. The protection voltage will then track the negative supply voltage and the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clipped to ground by diode forward conduction. Negative overvoltages are initially clipped close to the SLIC negative supply rail value. If sufficient current is available from the overvoltage, then the protector SCR will switch into a low voltage on-state condition. As the overvoltage subsides the high holding current of '61089 SCR avoids d.c. latchup.

The '61089 is intended to be used with a series resistance of at least 25 Ω and a suitable overcurrent function for Telcordia compliance. Power fault conditions require a series overcurrent element which either interrupts or reduces the circuit current before the '61089 current rating is exceeded. For equipment compliant to ITU-T recommendations K.20 or K.21 or K.45 only, the series resistor value is set by the coordination requirements. For coordination with a 400 V limit GDT, a minimum series resistor value of 10 Ω is recommended.

The '61089 buffered gate design reduces the loading on the SLIC supply during overvoltages caused by power cross and induction. The regular pin-out for surface mount and through-hole packages is a feed through configuration. Connection to the SLIC is made via the '61089, Ring through pins 4 - 5 and Tip through pins 1 - 8. A non-feed-through surface mount (D) package is available. This shunt (SD) version pin-out does not make duplicate connections to pin 5 and pin 8 which increases package creepage distance from ground of the other connections from about 0.7 mm to over 3 mm. High voltage ringing SLICs, with battery voltages below -100 V and down to -155 V, can be protected by the TISP61089B device. Details of this device are in the TISP61089B data sheet.

Absolute Maximum Ratings, -40 °C ≤ T_J ≤ 85 °C (Unless Otherwise Noted)

Rating		Symbol	Value	Unit
Repetitive peak off-state voltage, V_{GK} = 0	61089	V_{DRM}	-100	V
	'61089A		-120	
Repetitive peak gate-cathode voltage, V_{KA} = 0	61089	V_{GKRM}	-85	V
	'61089A		-120	
Non-repetitive peak on-state pulse current (see Notes 1 and 2)				
10/1000 μs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)		I_{PPSM}	30	A
5/320 μs (ITU-T K.20, K.21& K.45, K.44 open-circuit voltage wave shape 10/700 μs)			40	
1.2/50 μs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)			100	
2/10 μs (Telcordia (Bellcore) GR-1089-CORE, Issue 2, February 1999, Section 4)			120	
Non-repetitive peak on-state current, V_{GG} = -75 V, 50 Hz to 60 Hz (see Notes 1 and 2)				
0.1 s		I_{TSM}	11	A
1 s			4.8	
5 s			2.7	
300 s			0.95	
900 s			0.93	
Non-repetitive peak gate current, 1/2 μs pulse, cathodes commoned (see Notes 1 and 2)		I_{GSM}	+40	A
Operating free-air temperature range		T_A	-40 to +85	°C
Junction temperature		T_J	-40 to +150	°C
Storage temperature range		T_{stg}	-40 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with -40 °C ≤ T_J ≤ 85 °C. The surge may be repeated after the device returns to its initial conditions. Gate voltage ranges are -20 V to -75 V for the '61089 and -20 V to -100 V for the '61089A.

2. The rated current values may be applied either to the Ring to Ground or to the Tip to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of an individual terminal pair). Above 85 °C, derate linearly to zero at 150 °C lead temperature.

Recommended Operating Conditions

Component		Min	Typ	Max	Unit
C_G	Gate decoupling capacitor	100	220		nF
R_S	Series resistor for GR-1089-CORE first-level surge survival	25			Ω
	Series resistor for GR-1089-CORE first-level and second-level surge survival	40			Ω
	Series resistor for GR-1089-CORE intra-building port surge survival	8			Ω
	Series resistor for K.20, K.21 and K.45 coordination with a 400 V primary protector	10			Ω

Electrical Characteristics, T_J = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_D	Off-state current	$V_D = V_{DRM}$, V_{GK} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
$V_{(BO)}$	Breakover voltage	2/10 μs, I_{PP} = -56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			-57		V
		2/10 μs, I_{PP} = -100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			-60		
		1.2/50 μs, I_{PP} = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			-60		
		1.2/50 μs, I_{PP} = -96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			-64		
$V_{GK(BO)}$	Gate-cathode impulse breakover voltage	2/10 μs, I_{PP} = -56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			9		V
		2/10 μs, I_{PP} = -100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
		1.2/50 μs, I_{PP} = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
		1.2/50 μs, I_{PP} = -96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			16		
V_F	Forward voltage	I_F = 5 A, t_w = 200 μs				3	V
V_{FRM}	Peak forward recovery voltage	2/10 μs, I_{PP} = 56 A, R_S = 45 Ω, V_{GG} = -48 V, C_G = 220 nF			6		V
		2/10 μs, I_{PP} = 100 A, R_S = 50 Ω, V_{GG} = -48 V, C_G = 220 nF			8		
		1.2/50 μs, I_{PP} = 53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			8		
		1.2/50 μs, I_{PP} = 96 A, R_S = 52 Ω, V_{GG} = -48 V, C_G = 220 nF			12		
I_H	Holding current	I_T = -1 A, di/dt = 1A/ms, V_{GG} = -48 V		-150			mA
I_{GKS}	Gate reverse current	$V_{GG} = V_{GK} = V_{GKRM}$, V_{KA} = 0	T_J = 25 °C			-5	μA
			T_J = 85 °C			-50	μA
I_{GT}	Gate trigger current	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -48 V				5	mA
V_{GT}	Gate-cathode trigger voltage	I_T = -3 A, $t_{p(g)} \geq$ 20 μs, V_{GG} = -48 V				2.5	V
Q_{GS}	Gate switching charge	1.2/50 μs, I_{PP} = -53 A, R_S = 47 Ω, V_{GG} = -48 V, C_G = 220 nF			0.1		μC
C_{KA}	Cathode-anode off-state capacitance	f = 1 MHz, V_d = 1 V, I_G = 0, (see Note 3)	V_D = -3 V			100	pF
			V_D = -48 V			50	pF

NOTES: 3. These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

Parameter		Test Conditions		Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	T_A = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, P_{TOT} = 1.7 W	D Package			120	°C/W