Features

- **Low-voltage and Standard-voltage Operation**
  - **1.8v (V_{CC} = 1.8V to 3.6V)**
  - **2.5v (V_{CC} = 2.5V to 5.5V)**
- **Internally Organized 65,536 x 8**
- **Two-wire Serial Interface**
- **Schmitt Triggers, Filtered Inputs for Noise Suppression**
- **Bidirectional Data Transfer Protocol**
- **1 MHz (2.5V, 5.5V), 400 kHz (1.8V) Compatibility**
- **Write Protect Pin for Hardware and Software Data Protection**
- **128-byte Page Write Mode (Partial Page Writes Allowed)**
- **Self-timed Write Cycle (5 ms Max)**
- **High Reliability**
  - **Endurance: 1,000,000 Write Cycles**
  - **Data Retention: 40 Years**
- **Lead-free/Halogen-free Devices**
- **8-lead PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead TSSOP, 8-ball dBGA2, and 8-lead Ultra Thin Small Array (SAP) Packages**
- **Die Sales: Wafer Form, Waffle Pack and Bumped Die**

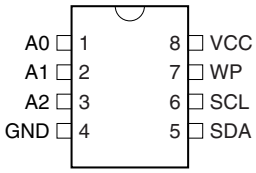
Description

The AT24C512B provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each. The device's cascadable feature allows up to eight devices to share a common two-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead EIAJ SOIC, 8-lead TSSOP, 8-ball dBGA2 and 8-lead Ultra Thin SAP packages. In addition, the entire family is available in 1.8V (1.8V to 3.6V) and 2.5V (2.5V to 5.5V) versions.

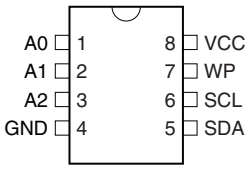
Table 0-1. Pin Configurations

Pin Name	Function
A0–A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect

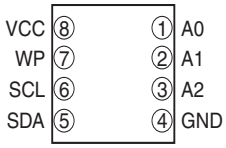
8-lead TSSOP



8-lead PDIP

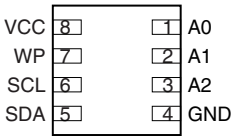


8-ball dBGA2



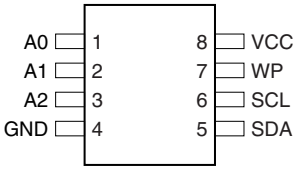
Bottom View

8-lead Ultra Thin SAP



Bottom View

8-lead SOIC



Two-wire Serial EEPROM

512K (65,536 x 8)

AT24C512B

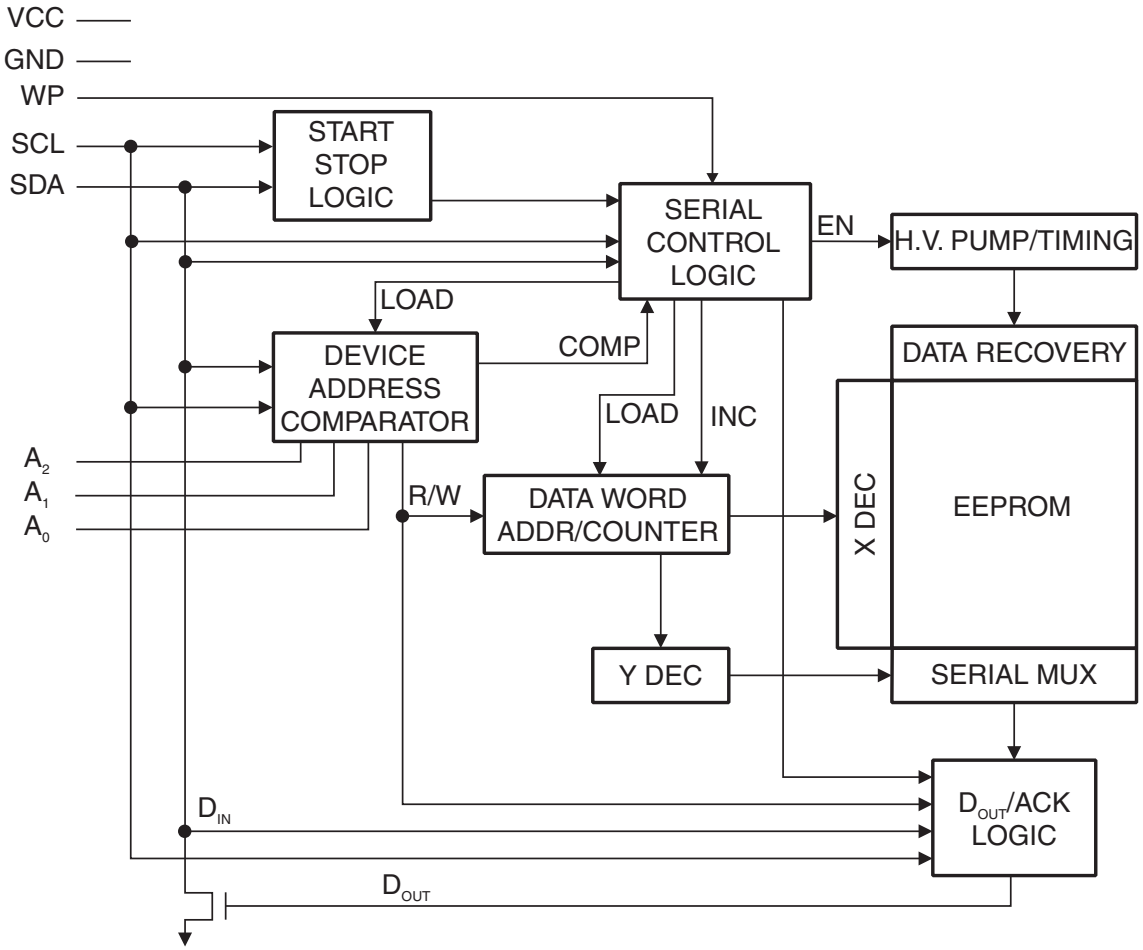
with Three Device Address Inputs

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-1. Block Diagram



2. Memory Organization

AT24C512B, 512K SERIAL EEPROM: The 512K is internally organized as 512 pages of 128-bytes each. Random word addressing requires a 16-bit data word address.

Table 2-1. Pin Capacitance[1]

Applicable over recommended operating range from: T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.8V to +5.5V

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 2-2. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		3.6	V
V_{CC2}	Supply Voltage			2.5		5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	READ at 400 kHz			2.0	mA
I_{CC}	Supply Current	V_{CC} = 5.0V	WRITE at 400 kHz			3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}			1.0	µA
		V_{CC} = 3.6V				3.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}			2.0	µA
		V_{CC} = 5.5V				6.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.05	3.0	µA
V_{IL}	Input Low Level[1]			–0.6		V_{CC} x 0.3	V
V_{IH}	Input High Level[1]			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Level	V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V
V_{OL2}	Output Low Level	V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 2-3. AC Characteristics (Industrial Temperature)

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, CL = 100 pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	1.8-volt		2.5, 5.0-volt		Units
		Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL		400		1000	kHz
t_{LOW}	Clock Pulse Width Low	1.3		0.4		µs
t_{HIGH}	Clock Pulse Width High	0.6		0.4		µs
t_i	Noise Suppression Time(1)		100		50	ns
t_{AA}	Clock Low to Data Out Valid	0.05	0.9	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	1.3		0.5		µs
$t_{HD.STA}$	Start Hold Time	0.6		0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		0.25		µs
$t_{HD.DAT}$	Data In Hold Time	0		0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
t_R	Inputs Rise Time(1)		0.3		0.3	µs
t_F	Inputs Fall Time(1)		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.6		0.25		µs
t_{DH}	Data Out Hold Time	50		50		ns
t_{WR}	Write Cycle Time		5		5	ms
Endurance(1)	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization only.

2. AC measurement conditions:
   R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5V), 10 kΩ (1.8V)
   Input pulse voltages: 0.3 V_{CC} to 0.7 V_{CC}
   Input rise and fall times: ≤ 50 ns
   Input and output timing reference voltages: 0.5 V_{CC}

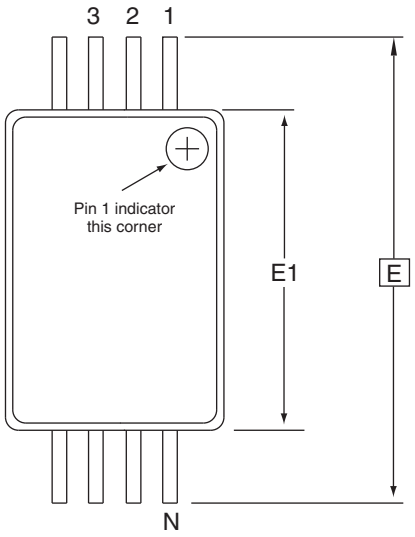
Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT24C512B-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT24C512B-PU25 (Bulk form only)	2.5	8P3	
AT24C512BN-SH-B[1] (NiPdAu Lead Finish)	1.8	8S1	
AT24C512BN-SH-T[2] (NiPdAu Lead Finish)	1.8	8S1	
AT24C512BN-SH25-B[1] (NiPdAu Lead Finish)	2.5	8S1	
AT24C512BN-SH25-T[2] (NiPdAu Lead Finish)	2.5	8S1	
AT24C512BW-SH-B[1] (NiPdAu Lead Finish)	1.8	8S2	
AT24C512BW-SH-T[2] (NiPdAu Lead Finish)	1.8	8S2	
AT24C512BW-SH25-B[1] (NiPdAu Lead Finish)	2.5	8S2	
AT24C512BW-SH25-T[2] (NiPdAu Lead Finish)	2.5	8S2	
AT24C512B-TH-B[1] (NiPdAu Lead Finish)	1.8	8A2	
AT24C512B-TH-T[2] (NiPdAu Lead Finish)	1.8	8A2	
AT24C512B-TH25-B[1] (NiPdAu Lead Finish)	2.5	8A2	
AT24C512B-TH25-T[2] (NiPdAu Lead Finish)	2.5	8A2	
AT24C512BY7-YH-T[2] (NiPdAu Lead Finish)	1.8	8Y7	
AT24C512BY7-YH25-T[2] (NiPdAu Lead Finish)	2.5	8Y7	
AT24C512BU2-UU-T[2]	1.8	8U2-1	
AT24C512B-W-11[3]	1.8	Die Sale	Industrial Temperature (–40°C to 85°C)

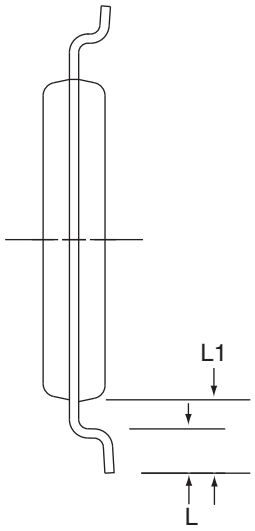
Notes:
1. "-B" denotes bulk
2. "-T" denotes tape and reel. SOIC = 4K per reel. TSSOP and dBGA2 = 5K per reel. SAP = 3K per reel. EIAJ = 2K per reel.
3. Available in tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.200" Wide Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8A2	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y7	8-lead, 6.00 mm x 4.90 mm Body, Ultra Thin, Dual Footprint, Non-leaded, Small Array Package (SAP)
8U2-1	8-ball, die Ball Grid Array Package (dBGA2)
Options	
–1.8	Low-voltage (1.8V to 3.6V)
–2.5	Low-voltage (2.5V to 5.5V)

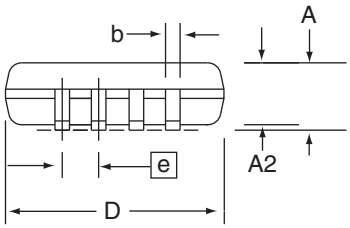
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B